PATENT ABSTRACTS OF JAPAN

(11)Publication number : 11-167373

(43)Date of publication of application : 22.06.1999

(51)Int.Cl. G09G 3/36
G02F 1/133
G02F 1/133
H01L 29/786
H01L 21/336

(21)Application number : 10-146613

(22)Date of filing : 11.05.1998

(71)Applicant : SEMICONDUCTOR ENERGY LAB CO LTD

(72)Inventor : KOYAMA JUN
OSAME MITSUAKI
ASAMI MUNEHIRO

(30)Priority

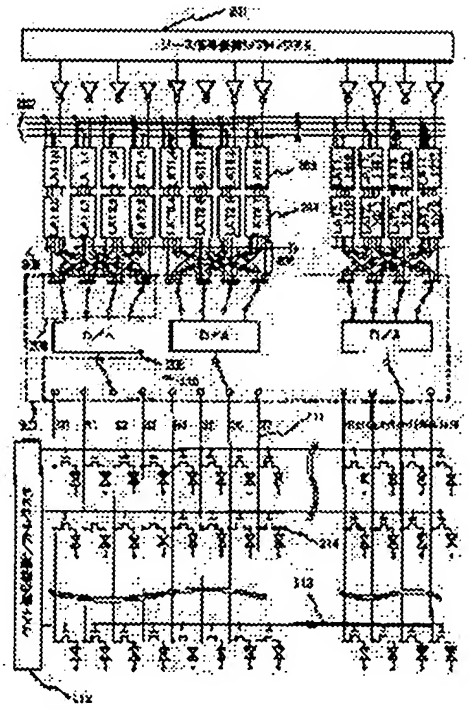
Priority number : 09286098 Priority date : 01.10.1997 Priority country : JP

(54) SEMICONDUCTOR DISPLAY DEVICE AND DRIVING METHOD THEREOF

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a semiconductor display device of a digital gradation system reduced in a driving circuit area.

SOLUTION: In a driving circuit of a semiconductor display device of a digital gradation system, one D/A conversion circuit 208 is arranged for plural source signal lines, each of which is driven by time sharing. Thus, the number of D/A conversion circuits 208 can be reduced, and miniaturization of the semiconductor display device is possible.



* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]
[0002] This invention relates to the semi-conductor display which displays information on an image etc. by the pixel arranged in the shape of a matrix.
[0003]
[Description of the Prior Art]
[0004] The semiconductor device, for example, the technique which produces a thin film transistor (TFT), in which the semi-conductor thin film was formed on the glass substrate cheap recently is progressing quickly. The reason is because the need of an active matrix liquid crystal display (liquid crystal panel) has increased.
[0005] TFT is arranged, respectively to the pixel field of dozens arranged in the shape of a matrix - 1 million numbers, and an active matrix liquid crystal panel controls the charge which frequents each pixel electrode by the switching function of TFT.
[0006] Also in it, the active matrix liquid crystal display of the digital gradation method in which a high-speed drive is possible has attracted attention.
[0007] The active matrix liquid crystal display of the conventional digital gradation method is shown in drawing 1 . The active matrix liquid crystal indicating equipment of the conventional digital gradation method is constituted by the source signal-line side shift register 101, the digital decoder 102, a latch circuit 103 (Local Area Transport1), a latch circuit 104 (Local Area Transport2), the latch pulse line 105, the D/A conversion circuit 106, the source signal line 107, the gate signal line side shift register 108, the gate signal line (scanning line) 109, the pixel TFT110, etc. as shown in drawing 1 .
[0008] The digital gradation signal supplied to the address lines 1-4 of the digital decoder 102 is written in Local Area Transport1 by the timing signal from a source signal-line side shift register.
[0009] Time amount until the writing of a digital gradation signal to Local Area Transport1 group is completed briefly is called an one-line period. That is, the time interval of the time of the writing of the gradation signal from a digital decoder being started to Local Area Transport1 by the side of the leftmost of drawing 1 to the time of the writing of the gradation signal from a digital decoder being completed to Local Area Transport1 of most right-hand side is an one-line period.
[0010] After the writing of a gradation signal to Local Area Transport1 group is completed, according to the timing of a shift register of operation, a latch pulse flows, and the gradation signal written in memory 1 group is sent out all at once to Local Area Transport2 group by latch pulse lines, and is written in them.
[0011] The writing of the gradation signal again supplied to a digital decoder is performed one by one in Local Area Transport1 group which finished sending out a gradation signal to Local Area Transport2 group by the signal from a source signal-line side shift register.
[0012] During the one-line period of eye this 2 order, a gradation electrical potential difference is chosen by the D/A conversion circuit (digital to analog circuit) according to the gradation signal sent out to

Local Area Transport2 group to compensate for initiation of the one-line period of eye 2 order.
[0013] The selected gradation electrical potential difference is supplied to the source signal line which corresponds during an one-line period.
[0014] By repeating the actuation mentioned above, the whole picture element part of a liquid crystal display is provided with an image.
[0015]
[Problem(s) to be Solved by the Invention]
[0016] However, in the case of the liquid crystal display of digital gradation which was mentioned above, in fact, the area of a D/A conversion circuit is quite large as compared with other circuits, and serves as hindrance of a miniaturization of the liquid crystal display desired in recent years.
[0017] Moreover, increase-izing of display capacity (display resolution) and highly minute-ization of display resolution have been attained with the rapid increment in the amount of information treated in recent years. However, the number of D/A conversion circuits will also increase with the increment in display capacity, and contraction of the area of the drive circuit section is desired eagerly.
[0018] Here, the number of pixels and a specification name show below the example of the display resolution of the computer generally used.
[0019]
The number of pixels (horizontal x length) : Specification name 640x400 : EGA 640x480 : VGA 800x600 : SVGA 1024x768 : XGA 1280x1024 : SXGA [0020] For example, when XGA specification (1024x768 pixels) is taken for an example, a D/A converter is needed in the drive circuit mentioned above for each to 1024 signal lines.
[0021] Moreover, recently, also in the field of a personal computer, since the software which performs two or more displays from which character differs on a display has spread, it is shifting to the display corresponding to XGA with still higher display resolution, or SXGA specification rather than VGA or SVGA specification.
[0022] Furthermore, a liquid crystal display with the above-mentioned high display resolution has come to be used also for the display of a television signal in addition to the display of the data signal in a personal computer.
[0023] In order to express beautiful image quality like Hi-Vision TV (HDTV) and an extended definition television (EDTV) in recent years, as compared with the conventional television, the image data of one screen is increasing several times. Moreover, improvement in conspicuousness, and since it becomes possible to display two or more images at one display, a big screen and the Takashina tone are needed increasingly with big screen-ization.
[0024] Moreover, as specification of the display resolution of TV (ATV) of future digital-broadcasting correspondence, 1920x1080 pixels is leading and the reductions of area of the drive circuit section are demanded immediately.
[0025] however, since the occupancy area of a D/A conversion circuit is large as mentioned above, the number of pixels increases -- it is alike, and it follows, and the area of the drive circuit section is boiled markedly, and becomes large, and this serves as hindrance of a miniaturization of a liquid crystal display.
[0026] Then, this invention is made in view of a problem which was mentioned above, decreases the area which a D/A conversion circuit shuts in the drive circuit section, and offers a small semi-conductor display, especially a liquid crystal display.
[0027]
[Means for Solving the Problem]
[0028] an operative condition with this invention -- if it depends like, it will be the semi-conductor indicating equipment equipped with the D/A conversion circuit section which has two or more D/A conversion circuits, and the semi-conductor indicating equipment with which each of two or more of said D/A conversion circuits carries out analogue conversion of the digital gradation signal supplied from a store circuit one by one will be offered. The above-mentioned purpose is attained by this.
[0029] Said store circuit may contain two or more latch circuits.

[0030] Moreover, the store circuit which memorizes m x bit digital gradation signals (m and x are the natural number) according to the embodiment with this invention, The D/A conversion circuit section which carries out analogue conversion of said m x bit digital gradation signals supplied from said store circuit, and supplies an analog signal to m source signal lines, It is a preparation ******** display. Said D/A conversion circuit section It has n D/A conversion circuits (n is the natural number), and each of said n D/A conversion circuits carries out analogue conversion of the x bit digital gradation signal of a m/n individual to order, and the semi-conductor display supplied to said source signal line of a corresponding m/n book is offered. The above-mentioned purpose is attained by this.
[0031] Said store circuit may contain two or more latch circuits.
[0032] moreover, an operative condition with this invention -- the step which will memorize m one-line x bit digital gradation signals (m and x are the natural number) if it depends like, and n every -- the drive approach of the semi-conductor display containing the step at which each of a D/A conversion circuit (n is the natural number) sends out said x bit digital gradation signal of a m/n individual to the source signal line of the m/n book which carries out analogue conversion and corresponds to order at an one-line period is offered. The above-mentioned purpose is attained by this.
[0033] moreover, an operative condition with this invention -- if it depends like, by the timing signal from a shift register, m x bit digital gradation signals (m and x are the natural number) will be sampled, and the drive approach of the semi-conductor display containing the step to memorize and the step which sends out a gradation electrical potential difference to the source signal line of the m/n book which n D/A conversion circuits (n is the natural number) carry out analogue conversion of said x bit digital gradation signal of a m/n individual one by one, and corresponds will be offered. The above-mentioned purpose is attained by this.
[0034]
[Example]
[0035] (Example 1)
[0036] In this example, reduction of the area which the D/A conversion circuit in a drive circuit occupies can be aimed at in the drive circuit by the side of a source signal line (driver) by preparing one D/A conversion circuit for every four source signal lines.
[0037] This example explains taking the case of the liquid crystal display which has the display resolution of 1920x1080. Drawing 2 R> 2 is referred to. The schematic diagram of the liquid crystal display of this example is shown in drawing 2 . 201 is a source signal-line side shift register, 202 is an address decoder, and a digital gradation signal is supplied to a latch circuit 203 (Local Area Transports [1 and 0] - Local Area Transports 1 and 1919). In addition, in this example, although the drive circuit of 4-bit digital gradation is mentioned as the example, this invention is not limited to this and may be applied to 6 bits, 8 bits, or the other digital gradation drive circuit.
[0038] 204 is a latch circuit (Local Area Transports 2 and 0 - Local Area Transports 2 and 1919), and memorizes the data sent out all at once based on the latch pulse from the latch pulse line 205 from the Local Area Transport1 group 1 and Local Area Transports 0 - Local Area Transports 1 and 1919. A signal line 206 supplies the gradation signal from the Local Area Transport2 group 2 and Local Area Transports 0 - Local Area Transports 2 and 1919 to the lower berth. In this example, since a 4-bit digital gradation signal is treated, the signal line 206 will have come out of each four Local Area Transports2 at a time. In addition, although a sign is attached to a signal line 206 in order, it is omitting in drawing 2 .
[0039] Drawing 14 carries out attention **** of the circuit from Local Area Transport2 to the source signal line 211 in drawing 2 at the D/A conversion circuit 208 of the leftmost of drawing 2 . a signal line 206 -- L0 and 0-L -- it turns out that 3 or 3 signs are attached. In the signs La and b which show a signal line 206, a shall follow the number of Local Area Transport2, b shall follow 0-3, and a high order bit - a lower bit shall be shown.
[0040] the same -- all signal lines -- L0 and 0-L -- 1919 or 3 signs are attached.
[0041] The part (broken-line section) shown by 207 is a D/A transducer, and is equipped with the D/A conversion circuit 208, the switching circuit 209 (broken-line section), and the switching circuit 210 (broken-line section). 211 is a source signal line and the sign of S0-S1919 is attached.

[0042] the D/A transducer 207 -- setting -- the D/A conversion circuit 208 -- every four (every [That is, the signal line L0 connected to the Local Area Transport2 group 2 and Local Area Transports 0 - Local Area Transports 2 and 1919, 0-L / of 1919 and 3] 16) of Local Area Transport2 -- and one source signal lines S0-S1919 are formed every four. Therefore, in this example, 480 D/A conversion circuits (= 1920/4) 208 will be formed. The switching circuit 209 connected to the D/A conversion circuit 208 of most left-hand side in drawing 2 makes sequential selection of the bit signal from one [2] of four Local Area Transports2, respectively. A switching circuit 210 chooses one of S0-S3.
[0043] 212 is a gate signal line side shift register, and supplies a scan signal to the scanning line 213. Moreover, 214 is Pixel TFT and constitutes a pixel with an electrode, a liquid crystal ingredient, etc.
[0044] Next, actuation of the semi-conductor display of this example is explained.
[0045] First, a digital gradation signal is written in Local Area Transport1 group from the digital decoder 202 one by one by the timing signal from the source signal-line side shift register 201.
[0046] Time amount until the writing of a digital gradation signal to Local Area Transport1 group is completed briefly is an one-line period. That is, the time interval of the time of the writing of the gradation signal from a digital decoder being started to Local Area Transports 1 and 0 by the side of the leftmost of drawing 1 to the time of the writing of the gradation signal from a digital decoder being completed to Local Area Transports 1 and 1919 of most right-hand side is an one-line period.
[0047] After the writing of a gradation signal to Local Area Transport1 group is completed, the gradation signals written in Local Area Transport1 group are sent out to Local Area Transport2 group all at once according to the latch pulse supplied to the latch pulse line 205. Local Area Transport2 group memorizes a gradation signal and is a story [0048] to a signal line 206. The writing of the gradation signal again supplied to the digital decoder 202 is performed one by one in Local Area Transport1 group which finished sending out a gradation signal to Local Area Transport2 group by the signal from the source signal-line side shift register 201.
[0049] Next, actuation until the gradation signal supplied to a signal line 206 is changed into a gradation electrical potential difference by the D/A conversion circuit section 207 and is sent out to the source signal lines S0-S1919 one by one is explained taking the case of the switching circuit 209 located most on left-hand side in drawing 2 , the D/A conversion circuit 208, and a switching circuit 210.
[0050] Drawing 14 is referred to again. The D/A transducer 207 during the one-line period when the gradation signal is again written in Local Area Transport1 group one by one an one-line period -- quadrisecting -- four switches of a switching circuit 209 -- a signal line L0 and 0-L -- 0, 3, L1, and 0-L -- 1, 3, L2, and 0-L -- 2, 3, L3, and 0-L -- sequential connection is made to 3 and 3, and sequential connection of the switching circuit 210 is made to S0-S3. that is, four switches of during the first quadrant Rhine period and a switching circuit 209 -- L0 from Local Area Transports 2 and 0, and 0-L -- choosing [and] 0 and 3 as coincidence, 210 chooses a switching circuitS0. After the gradation signal supplied to Local Area Transports 2 and 0 in the meantime is inputted into 4-bit coincidence at the D/A conversion circuit 208 and analogue conversion is carried out by the D/A conversion circuit 208, it serves as a gradation electrical potential difference, and is sent out to S0. on the other hand -- during this period -- the signal line L1 from Local Area Transports 2 and 1 - Local Area Transports 2 and 3, and 0-L -- although a gradation signal is continuing being supplied to 3 and 3 -- a switching circuit 209L1 and 0-L -- 3 and 3 are not chosen. Moreover, a switching circuit 210 does not choose S1-S3 in the meantime.
[0051] next, four switches of during the next quadrant Rhine period and a switching circuit 209 -- L1 from Local Area Transports 2 and 1, and 0-L -- choosing [and] 1 and 3 as coincidence, 210 chooses a switching circuitS1. After the gradation signal supplied to Local Area Transports 2 and 1 in the meantime is changed into a gradation electrical potential difference by the D/A conversion circuit 208, it is sent out to S1. on the other hand -- during this period -- the signal line L0 from Local Area Transports 2 and 0, Local Area Transports 2 and 2, and Local Area Transports 2 and 3, and 0-L -- 0, 3, L2, and 0-L -- 2, 3 and L3, and 0-L, although a gradation signal is continuing being supplied to 3 and 3 a switching circuit 209 -- L0 and 0-L -- 0, 3, L2, and 0-L -- 2, 3 and L3, and 0-L -- 3 and 3 are not chosen. Moreover, a switching circuit 210 does not choose S0, S2, and S3 in the meantime.
[0052] furthermore, four switches of during the next quadrant Rhine period and a switching circuit 209 -

- L2 from Local Area Transports 2 and 2, and 0-L -- choosing [and] 2 and 3 as coincidence, 210 chooses a switching circuitS2. After the gradation signal supplied to Local Area Transports 2 and 2 in the meantime is changed into a gradation electrical potential difference by the D/A conversion circuit 208, it is sent out to S2. on the other hand -- during this period -- the signal line L0 from Local Area Transports 2 and 0, Local Area Transports 2 and 1, and Local Area Transports 2 and 3, and 0-L -- 0, 3, L1, and 0-L -- 1, 3 and L3, and 0-L, although a gradation signal is continuing being supplied to 3 and 3 a switching circuit 209 -- L0 and 0-L -- 0, 3, L1, and 0-L -- 1, 3 and L3, and 0-L -- 3 and 3 are not chosen. Moreover, a switching circuit 210 does not choose S0, S1, and S3 in the meantime.

[0053] furthermore, four switches of during the next quadrant Rhine period (that is, during the quadrant Rhine period of the last of an one-line period), and a switching circuit 209 -- L3 from Local Area Transports 2 and 3, and 0-L -- choosing [and] 3 and 3 as coincidence, 210 chooses a switching circuitS3. After the gradation signal supplied to Local Area Transports 2 and 3 in the meantime is changed into a gradation electrical potential difference by the D/A conversion circuit 208, it is sent out to S3. on the other hand -- during this period -- the signal line L0 from Local Area Transports 2 and 0 - Local Area Transports 2 and 2, and 0-L -- 0, 3, L1, and 0-L -- 1, 3 and L2, and 0-L -- although a gradation signal is continuing being supplied to 2 and 3 -- a switching circuit 209 -- L0 and 0-L -- 0, 3, L1, and 0-L -- 1, 3 and L2, and 0-L -- 2 and 3 are not chosen. Moreover, a switching circuit 210 does not choose S0-S2 in the meantime.

[0054] By actuation mentioned above, a gradation electrical potential difference is sent out to the source signal lines S0-S3 in order of a quadrant Rhine period every. By the gradation electrical potential difference sent out to this source signal line, and the scan signal supplied to the scanning line 213 from the gate signal line side shift register 212, an electrical potential difference is impressed to Pixel TFT one by one, and a pixel is switched.

[0055] Actuation mentioned above is performed to coincidence about every four of all Local Area Transports 2 and 0 - Local Area Transports 2 and 1919.

[0056] Since the writing of the new gradation signal to Local Area Transport1 group is completed when sending out of the gradation electrical potential difference to the source signal line of an one-line period is completed, the gradation signals written in Local Area Transport1 group are again sent out to Local Area Transport2 group all at once by the latch pulse from the latch pulse line 205. Local Area Transport2 group memorizes a new gradation signal and continues supplying a gradation signal to a signal line 206.

[0057] and 206 signal lineL0 by the switching circuit 209 and switching circuit 210 which were mentioned above and 0-L -- selection of 3, 3, and source signal-line S0-1919 is started.

[0058] The timing of the data sent out to the source signal lines S0-S1919 is shown in drawing 3 . In addition, in fact, although the analog gradation electrical potential difference is impressed to the source signal lines S0-S1919, in drawing 3 , only the timing to which a gradation electrical potential difference is supplied is shown.

[0059] The above-mentioned actuation is performed about all the selected scanning lines, and the image of one screen is created. Creation of this one screen is performed 60 times in 1 second.

[0060] Here, the circuitry of the D/A transducer 207 is explained with reference to drawing 4 . In drawing 4 , for convenience, although only the switching circuit 209 of most left-hand side, the D/A conversion circuit 208, and the switching circuit 210 are shown in drawing 2 , 480 circuits of explanation which have the same configuration as these are prepared. Moreover, the expedient top of explanation and the switching circuit 209 are shown by the logical circuit notation. Moreover, since a well-known D/A conversion circuit may be used for the D/A conversion circuit 208, it omits here.

[0061] A switching circuit 209 includes 2 input NAND circuit (N0-N15) of four signal lines [3 or 16] LS0-LS, and four 4 input NAND circuits (4inN0-4inN3). Moreover, a switching circuit 210 contains four analog switches (ASW0-ASW3) which consist of eight signal lines SS0-SS3 and reversal SS 0 - reversal SS 3, an N channel mold TFT, and a P channel mold TFT. In addition, the reversal signal of the signal sent out to signal lines SS0-SS3 is sent out to the signal-line reversal SS 0 - reversal SS 3.

[0062] it is shown in drawing 4 -- as -- the signal line L0 from Local Area Transport2 group, and 0-L --

3, 3, and signal lines LS0-LS3 have inputted into the 2 input NAND (N0-N15), respectively. The output of these 16 2 inputs NAND has inputted into four 4 inputs NAND (4inN0-4inN3).
[0063] The output of four 4 inputs NAND is inputted into the D/A conversion circuit 208.
[0064] The output from the D/A conversion circuit 208 is inputted into four analog switches (ASW0-ASW3). Four analog switches are controlled by signal lines SS0-SS3 and the signal from reversal SS 0 - reversal SS 3.
[0065] The above configurations are prepared every four of all Local Area Transports2 (Local Area Transports [2 and 0] - Local Area Transports 2 and 1919).
[0066] The timing chart of the signal inputted into each signal line is shown in drawing 5 . A 4-bit digital gradation signal is inputted into Local Area Transport2 group (Local Area Transports 2 and 0 - Local Area Transports 2 and 1919). The gradation signal inputted into Local Area Transport2 group is rewritten by the new gradation signal for every one-line period.
[0067] Since the signal of Hi is inputted into LS0-LS3 in order of a quadrant Rhine period every, the 4-bit digital gradation signal supplied to Local Area Transport2 group will be inputted into the D/A conversion circuit 208 in order of a quadrant Rhine period every.
[0068] Analogue conversion of the digital gradation signal inputted into the D/A conversion circuit 208 is carried out, it serves as a gradation electrical potential difference, and is inputted into the analog switches ASW0-ASW3 of the lower berth. Analog switches ASW0-ASW3 are controlled by signal lines SS0-SS3 and the reversal signal lines SS0-SS3 of those. By opening analog switches ASW0-ASW3 in order, a gradation electrical potential difference is supplied to the source signal lines S0-S3 in order of a quadrant Rhine period every.
[0069] The above actuation is performed about the gradation signal from all Local Area Transport2 groups, and a gradation electrical potential difference is sent out to all corresponding source signal lines. In addition, in fact, although the analog gradation electrical potential difference is impressed to the source signal lines S0-S1919, in drawing 3 , only the timing to which a gradation electrical potential difference is supplied is shown.
[0070] Thus, lighting of the pixel TFT for one line is performed. And the above actuation is performed about all the selected scanning lines (1080), and the image of one screen (one frame) is created. Creation of this one screen is performed 60 times in 1 second.
[0071] In this example, since creation of one screen is performed 60 times in 1 second, one-frame periods are 1/60=16.7msec. Moreover, the periods which an one-line period serves as 1/60/1080= 15.4microsec, and drive each pixel are 1/60/1080/4= 3.86microsec. As a property required of the pixel TFT which can realize such a high-speed drive, they are more than carrier mobility of 30cm 2 / Vs. The following examples 2 show the manufacture approach of a semiconductor device that such highly efficient TFT is realizable.
[0072] Since the number of the D/A conversion circuits which occupy a big area also in a drive circuit can be made into the conventional quadrant according to the drive circuit of this example, even if it takes the increment for a switching circuit into consideration, the miniaturization of a semi-conductor display is realizable.
[0073] In addition, in this example, although the number of D/A conversion circuits was made into the conventional quadrant, this invention can also make the number of D/A conversion circuits numbers other than this. For example, when one D/A conversion circuit per eight source signal lines is assigned, in the semi-conductor display of this example, the number of D/A conversion circuits becomes 240 pieces, and the further reductions of area of a drive circuit are realized. Thus, it is not limited to this example whether one D/A conversion circuit per how many source signal lines is assigned.
[0074] therefore, when the semi-conductor display of this invention has m source signal lines (m is the natural number) (if it puts in another way -- the number of pixels (horizontal x length) -- mx -- arbitrary cases), as one line, m x bit digital gradation signals (x is the natural number) are supplied. in this case -- if the semi-conductor display of this invention considers as D/A conversion circuit section preparation ****** which has n D/A conversion circuits (n is the natural number) -- every -- D / A conversion circuit will carry out analogue conversion of the digital gradation signal of a m/n individual one by one,

and will carry out sequential supply of the analog signal to the source line of a corresponding m/n book. In addition, what is necessary is just to use the D/A conversion circuit according to the number of bits of a digital gradation signal.

[0075] (Example 2)

[0076] This example explains the making process of the liquid crystal display which has the drive circuit used in the example 1.

[0077] By this example, two or more TFT(s) are formed on the substrate which has an insulating front face, and the example which constitutes a pixel matrix circuit and a circumference circuit including a drive circuit in a monolithic is shown in drawing 6 - drawing 9 R> 9. In addition, this example shows the CMOS circuit which is a basic circuit as an example of circumference circuits, such as a drive circuit. moreover, although it is alike, it attaches and the making process is explained by this example when the P channel mold TFT and N channel mold TFT are equipped with one gate electrode, respectively, the CMOS circuit by TFT equipped with two or more gate electrodes like a double-gate mold is producible similarly.

[0078] Drawing 6 is referred to. First, the quartz substrate 601 is prepared as a substrate which has an insulating front face. The silicon substrate which formed the thermal oxidation film instead of the quartz substrate can also be used. Moreover, it is very good in an approach which once forms the amorphous silicon film on a quartz substrate, oxidizes it thermally completely, and is made into an insulator layer. Furthermore, the quartz substrate, ceramic substrate, or silicon substrate which formed the silicon nitride film as an insulator layer may be used.

[0079] 602 is the amorphous silicon film, and it is adjusted so that final thickness (thickness in consideration of the film decrease after thermal oxidation) may be set to 10-75nm (preferably 15-45nm). In addition, it is important to manage high impurity concentration in the film thoroughly on the occasion of membrane formation.

[0080] In addition, it is important to manage high impurity concentration in the film thoroughly on the occasion of membrane formation of the amorphous silicon film. the concentration of C (carbon) and N (nitrogen) which are the impurity which checks crystallization in the amorphous silicon film 602 in the case of this example -- each -- 5x1018 atoms/cm3 -- the following (it is 5x1017 atoms/cm3 typically hereafter) It is 2x1017 atoms/cm3 preferably. The following and O (oxygen) are 1.5x1019 atoms/cm3. It manages so that it may become the following (typically 1x1018 atoms/cm3 following, preferably 5x1017 atoms/cm3 henceforth). It is because it will become the cause of doing a bad influence in the case of next crystallization, and reducing the membraneous quality after crystallization if each impurity exists by the concentration beyond this. The above-mentioned impurity element concentration in the film is defined [be / it / under / this / specification / setting] by the minimum value in the measurement result of SIMS (secondary mass ion analysis).

[0081] In order to obtain the above-mentioned configuration, as for the reduced pressure heat CVD furnace used by this example, it is desirable to perform dry cleaning periodically and to attain defecation of a membrane formation room. Dry cleaning is ClF3 of 100 - 300sccm in the furnace heated at about 200-400 degrees C. What is necessary is just to clean a membrane formation room with the fluorine which generated gas (chlorine fluoride) by the sink and the pyrolysis.

[0082] In addition, according to this invention persons' knowledge, 300 degrees C costs whenever [furnace temperature], and it is ClF3. When the flow rate of gas (chlorine fluoride) is set to 300sccm(s), the affix (the principal component of the silicon is mainly carried out) of about 2-micrometer thickness can be removed completely in 4 hours.

[0083] Moreover, the hydrogen concentration in the amorphous silicon film 602 is also a very important parameter, and is the appearance from which the film with crystallinity with it more sufficient [to stop a hydrogen content low] is obtained. Therefore, as for membrane formation of the amorphous silicon film 602, it is desirable that it is a reduced pressure heat CVD method. In addition, it is also possible to use a plasma-CVD method by optimizing membrane formation conditions.

[0084] Next, the crystallization process of the amorphous silicon film 602 is performed. A technique given in JP,7-130652,A is used as a means of crystallization. Although which means of the example 1 of

this official report and an example 2 may be used, in this example, it is desirable to use the technical contents (detailed to JP,8-78329,A) indicated in the example 2 of these public relations.
[0085] A technique given in JP,8-78329,A forms the mask insulator layer 603 which chooses the addition field of a catalyst element first. The mask insulator layer 603 has two or more openings, in order to add a catalyst element. The location of this opening can determine the location of a crystalline region.
[0086] And the solution which contained nickel (nickel) as a catalyst element which promotes crystallization of the amorphous silicon film is applied with a spin coat method, and nickel content layer 604 is formed. In addition, as a catalyst element, cobalt (Co), iron (Fe), palladium (Pd), germanium (germanium), platinum (Pt), copper (Cu), gold (Au), etc. can be used besides nickel (drawing 6 (A)).
[0087] Moreover, the ion-implantation or the plasma doping method for having used the resist mask can also be used for the addition process of the above-mentioned catalyst element. In this case, since reduction of the occupancy area of an addition field and control of the growth distance of a horizontal growth field become easy, it becomes an effective technique in case the circuit made detailed is constituted.
[0088] Next, if the addition process of a catalyst element is completed, heat-treatment of 4 - 24 hours will be added by 450 degrees C at the temperature of 500-700 degrees C (typically 550-650 degrees C) into after hydrogen **** of about 1 hour, an inert atmosphere, a hydrogen ambient atmosphere, or an oxygen ambient atmosphere, and the amorphous silicon film 602 will be crystallized. At this example, nitrogen-gas-atmosphere mind performs heat-treatment of 14 hours at 570 degrees C.
[0089] At this time, crystallization of the amorphous silicon film 602 advances preferentially from the nucleus generated in the fields 605 and 606 which added nickel, and the crystalline regions 607 and 608 which grew almost in parallel to the substrate side of a substrate 601 are formed. These crystalline regions 607 and 608 are called a horizontal growth field. Since the crystals of each [the condition of having gathered comparatively] have gathered, a horizontal growth field has the advantage of excelling in overall crystallinity (drawing 6 (B)).
[0090] In addition, also when the technique indicated by the example 1 of above-mentioned JP,7-130652,A is used, the horizontal growth field and the field which can be called are formed microscopically. However, since karyogenesis happens to an ununiformity into a field, there is difficulty in respect of the controllability of the grain boundary.
[0091] If the heat-treatment for crystallization is completed, the mask insulator layer 603 will be removed, patterning will be performed, and the island-shape semi-conductor layers (barrier layer) 609, 610, and 611 which become in the horizontal growth fields 607 and 608 will be formed (drawing 6 (C)).

[0092] The barrier layer of N type TFT with which 609 constitutes a CMOS circuit here, the barrier layer of P type TFT with which 610 constitutes a CMOS circuit, and 611 are the barrier layers of N type TFT (pixel TFT) which constitutes a pixel matrix circuit.
[0093] If barrier layers 609, 610, and 611 are formed, the gate dielectric film 612 which comes by the insulator layer containing silicon on it will be formed.
[0094] And heat-treatment (gettering process of a catalyst element) for removing or reducing a catalyst element (nickel), as shown in drawing 6 (D) below is performed. This heat-treatment includes a halogen in a processing ambient atmosphere, and uses the gettering effectiveness of the metallic element by the halogen.
[0095] In addition, in order to fully acquire the gettering effectiveness by the halogen, it is desirable to perform the above-mentioned heat-treatment at the temperature exceeding 700 degrees C. Below at this temperature, disassembly of the halogenated compound in a processing ambient atmosphere becomes difficult, and there is a possibility that the gettering effectiveness may no longer be acquired.
[0096] Therefore, in this example, this heat-treatment is performed at the temperature exceeding 700 degrees C, it considers as 800-1000 degrees C (typically 950 degrees C) preferably, and the processing time is typically set to 0.5-1hr 0.1 to 6 hr.
[0097] In addition, this example shows the example which performs heat-treatment for 30 minutes at

950 degrees C into the ambient atmosphere which made the hydrogen chloride (HCl) contain [be / it / under / oxygen ambient atmosphere / receiving] by the concentration of 0.5 - 10 volume % (this example three volume %). If HCl concentration is carried out to more than the above-mentioned concentration, since the irregularity of thickness extent arises on the front face of barrier layers 609, 610, and 611, it is not desirable.

[0098] moreover -- although the compound was carried out and the example containing a halogen using HCl gas was shown -- as the other gas -- typical -- HF, NF3, HBr, Cl2, ClF3, BCl3, F2, and Br2 etc. -- a kind or two or more sorts of things chosen from the compound containing a halogen can be used.

[0099] In this process, gettering of barrier layers 609 and 610 and the nickel in 611 is carried out by operation of chlorine, it becomes an volatile nickel chloride and it is thought that it is broken away and removed into atmospheric air. And the concentration of barrier layers 609 and 610 and the nickel in 611 is 5x1017 atoms/cm3 by this process. It decreases even below.

[0100] In addition, 5x1017 atoms/cm3 The value to say is the minimum limit of detection of SIMS (mass secondary ion analysis). As a result of analyzing TFT which this invention persons made as an experiment, it is 1x1018 atoms/cm3. Below (it is 5x1017 atoms/cm3 preferably following), the effect of nickel to a TFT property was not checked. However, it is defined as the high impurity concentration in this specification being also for the minimum value of the measurement result of SIMS analysis.

[0101] Moreover, by the interface of barrier layers 609, 610, and 611 and gate dielectric film 612, a thermal oxidation reaction advances by the above-mentioned heat-treatment, and only the part of the thermal oxidation film increases the thickness of gate dielectric film 612. Thus, if the thermal oxidation film is formed, a semi-conductor / insulator layer interface with very little interface state density can be acquired. Moreover, there is effectiveness which prevents poor formation (edge thinning) of the thermal oxidation film in a barrier layer edge.

[0102] Moreover, after removing the mask insulator layer 603 for the gettering process of a catalyst element, a barrier layer may be performed before pattern NINGU. Moreover, the gettering process of a catalyst element may be performed after carrying out pattern NINGU of the barrier layer. Moreover, you may carry out combining which gettering process.

[0103] Furthermore, after performing heat-treatment in the above-mentioned halogen ambient atmosphere, it is also effective to aim at improvement in the membraneous quality of gate dielectric film 612 by performing heat-treatment of about 1 hour at 950 degrees C in nitrogen-gas-atmosphere mind.

[0104] In addition, the halogen used for gettering processing into barrier layers 609 and 610 and 611 by SIMS analysis is 1x1015 atoms/cm3 - 1x1020 atoms/cm3. Remaining by concentration is also checked. Moreover, it is confirmed by SIMS analysis in that case that the above-mentioned halogen is distributed at high concentration between barrier layers 609, 610, and 611 and the thermal oxidation film formed of heat-treatment.

[0105] Moreover, as a result of performing SIMS analysis about other elements, each C (carbon), N (nitrogen), O (oxygen), and S (sulfur) which are a typical impurity are 5x1018 atoms/cm3. It was checked that it is the following (it is 1x1018 atoms/cm3 typically following).

[0106] Next, the metal membrane which uses as a principal component the aluminum which is not illustrated is formed, and the patterns 613, 614, and 615 of a next gate electrode are formed by patterning. In this example, the aluminum film containing a 2wt(s)% scandium is used (drawing 7 (A)).

[0107] In addition, the polycrystal silicon film with which the impurity was added by the gate electrode may be used instead of the metal membrane which uses this aluminum as a principal component.

[0108] Next, the porous oxide films on anode 616, 617, and 618, the imperforation oxide films on anode 619, 620, and 621, and the gate electrodes 622, 623, and 624 are formed with a technique given in JP,7-135318,A (drawing 7 (B)).

[0109] In this way, if the condition of drawing 7 (B) is acquired, gate dielectric film 612 will be etched next by using the gate electrodes 622, 623, and 624 and the porous anodized films 616, 617, and 618 as a mask. And the porous oxide films on anode 616, 617, and 618 are removed, and the condition of drawing 7 (C) is acquired. In addition, it is gate dielectric film after processing that drawing 7 (C) is shown by 625, 626, and 627.

[0110] Next, the addition process of the impurity element which gives 1 conductivity is performed. What is necessary is just to use B (boron) or Ga (gallium), if it is N type as an impurity element and is P (Lynn) or As (arsenic), and P type.
[0111] In this example, impurity addition is divided into 2 times of processes, and is performed. First, 1st impurity addition (P (Lynn) is used in this example) is performed with high acceleration voltage 80keV extent, and it is n. - A field is formed. This n - For a field, P ion concentration is 1x1018 atoms/cm3 - 1x1019 atoms/cm3. It adjusts so that it may become.
[0112] Furthermore, 2nd impurity addition is performed with low acceleration voltage 10ke V extent, and it is n+. A field is formed. Since acceleration voltage is low at this time, gate dielectric film functions as a mask. Moreover, this n+ A field is adjusted so that sheet resistance may be set to 500ohms or less (preferably 300ohms or less).
[0113] The source field 628 of N type TFT which constitutes a CMOS circuit, the drain field 629, the low concentration impurity range 630, and the channel formation field 631 are formed through the above process. Moreover, the source field 632 of N type TFT which constitutes Pixel TFT, the drain field 633, the low concentration impurity range 634, and the channel formation field 635 are decided (drawing 7 R> 7 (D)).
[0114] In addition, the barrier layer of P type TFT which constitutes a CMOS circuit from a condition which shows in drawing 7 (D) also has the same composition as the barrier layer of N type TFT.
[0115] Next, as shown in drawing 8 (A), N type TFT is covered, the resist mask 636 is formed, and the impurity ion (boron is used in this example) which gives P type is added.
[0116] Although this process as well as the above-mentioned impurity addition process is performed in 2 steps, in order to make P type reverse N type, B (boron) ion of the concentration which is about several times the addition concentration of the above-mentioned P ion is added.
[0117] In this way, the source field 637 of P type TFT which constitutes a CMOS circuit, the drain field 638, the low concentration impurity range 639, and the channel formation field 640 are formed (drawing 8 (A)).
[0118] If a barrier layer is completed as mentioned above, impurity ion will be activated with combination, such as furnace annealing, laser annealing, and lamp annealing. The damage on a barrier layer received in it and coincidence at the addition process is also restored.
[0119] Next, after forming the cascade screen of the oxidation silicon film and a silicon nitride film as an interlayer insulation film 641 and forming a contact hole, the condition which the source electrodes 642, 643, and 644 and the drain electrodes 645 and 646 are formed, and shows in drawing 8 (B) is acquired. In addition, the organic nature resin film can also be used as an interlayer insulation film 641.
[0120] If the condition which shows in drawing 8 (B) is acquired, the meeting interlayer insulation film 647 which consists of organic nature resin film will be formed in the thickness of 0.5-3 micrometers. Polyimide, an acrylic, polyimidoamide, etc. are used as organic nature resin film. Since the point for the membrane formation approach that the advantage of the organic nature resin film is simple, the point which can thicken thickness easily, and specific inductive capacity are low, the point that parasitic capacitance can be reduced, a point excellent in surface smoothness, etc. are mentioned.
[0121] Next, the black mask 648 which becomes by the film which has protection-from-light nature is formed on an interlayer insulation film 647 at the thickness of 100nm. In addition, in this example, although the titanium film is used as a black mask 648, the resin film containing a black pigment etc. can also be used.
[0122] If the black mask 648 is formed, either or those cascade screens of the oxidation silicon film, a silicon nitride film, and the organic nature resin film will be formed in the thickness of 0.1-0.3 micrometers as an interlayer insulation film 649. And a contact hole is formed in an interlayer insulation film 647 and an interlayer insulation film 649, and the pixel electrode 650 is formed in the thickness of 120nm. According to the configuration of this example, auxiliary capacity is formed in the field which the black mask 648 and a pixel electrode superimpose (drawing 8 (C)). In addition, since this example is an example of the liquid crystal display of a transparency mold, it uses transparence electric conduction film, such as ITO, as electric conduction film which constitutes the pixel electrode 650.

[0123] Next, the whole substrate is heated in a 350-degree C hydrogen ambient atmosphere for 1 to 2 hours, and the dangling bond (azygos joint hand) in the film (especially inside of a barrier layer) is compensated with hydrogenating the whole component. A CMOS circuit and a pixel matrix circuit are producible on the same substrate through the above process.
[0124] Next, as shown in drawing 9 , the process which produces a liquid crystal panel is explained based on the active-matrix substrate produced by the above-mentioned process.
[0125] The orientation film 651 is formed in the active-matrix substrate of the condition of drawing 8 (C). Polyimide was used for the orientation film 651 in this example. Next, an opposite substrate is prepared. An opposite substrate consists of a glass substrate 652, transparence electric conduction film 653, and orientation film 654.
[0126] In addition, in this example, polyimide film in which a liquid crystal molecule carries out orientation in parallel to a substrate was used for the orientation film. In addition, it was made to carry out parallel orientation by performing rubbing processing with the fixed pre tilt angle with a liquid crystal molecule after orientation film formation.
[0127] In addition, although a color filter etc. is formed in an opposite substrate if needed, it omits here.
[0128] Next, the active-matrix substrate and opposite substrate which passed through the above-mentioned process are stuck through a sealant, a spacer (not shown), etc. according to a well-known cel **** process. Then, the liquid crystal ingredient 655 is poured in among both substrates, and it closes completely with encapsulant (not shown). Therefore, the liquid crystal panel of a transparency mold as shown in drawing 9 is completed.
[0129] in addition, in this example, the liquid crystal panel was made to display with TN (the twist -- nematic) mode. Therefore, with the cross Nicol's prism (condition one pair of polarizing plates make condition and each polarization shaft cross at right angles), one pair of polarizing plates (not shown) have been arranged so that a liquid crystal panel may be pinched.
[0130] Therefore, in this example, when the electrical potential difference is not impressed to the liquid crystal panel, displaying by the so-called normally white mode used as a white display is understood.
[0131] Moreover, the appearance of the produced liquid crystal panel is simplified and shown in drawing 10 R> 0 (A) - (C). As for a quartz substrate and 1002, in drawing 10 , 1001 is [a pixel matrix circuit and 1003] a source signal-line side drive circuit and the logical circuit of others [1004 / 1005 / a gate signal line side drive circuit and]. 1006 is an opposite substrate and 1007 is a FPC (FlexiblePrint Circuit) terminal. Moreover, drawing 10 (B) is drawing which looked at the liquid crystal panel of this example from the direction of an arrow head A in drawing 10 (A), and drawing 10 (C) is drawing seen from the direction of an arrow head B.
[0132] Although a logical circuit 1005 includes all the logical circuits that consist of TFT(s) in wide sense, in order to distinguish from the circuit currently called from the former the pixel matrix circuit and the drive circuit here, the other digital disposal circuits (a LCD controller, memory, pulse generator, etc.) are pointed out.
[0133] In addition, the active-matrix substrate has come only out of the end face in which the liquid crystal panel of this example attaches FPC outside at drawing 10 (B) and (C). It is understood that the three remaining end faces have gathered.
[0134] The photograph of the active matrix liquid crystal display of this example is shown in drawing 19 . According to drawing 19 , it turns out that the display of good check pattern is performed.
[0135] Here, the semi-conductor thin film produced by the production approach of this example is explained. According to the production approach of this example, the amorphous silicon film can be crystallized and the crystal silicone film called continuous grain boundary crystal silicon (the so-called Continuous Grain Silicon:CGS) can be obtained.
[0136] The horizontal growth field of the semi-conductor thin film obtained by the production approach of this example being cylindrical or the unique crystal structure which consists of the aggregate of a flat cylindrical crystal is shown. The description is shown below.
[0137] [Knowledge about the crystal structure of a horizontal growth field]
[0138] if it sees on the target of this example, it has the crystal structure to which two or more

cylindrical (or flat -- cylindrical) crystals were mutually located in a line with outline parallel with the regularity to the specific direction. This can be easily checked by observation by TEM (transmission electron microscopy).

[0139] Moreover, these people observed in the detail the grain boundary of the semi-conductor thin film obtained by the production approach of this example mentioned above by HR-TEM (high-resolution transmission electron microscopy) (drawing 19). however, it is defined as what points out the grain boundary formed in the boundary where cylindrical crystals which are different unless the grain boundary has a notice in this detail in the letter touched. It follows, for example, thinks in distinction from the grain boundary in macroscopic semantic **** in which a separate horizontal growth field collides and is formed.

[0140] By the way, above-mentioned HR-TEM (high-resolution transmission electron microscopy) is the technique of irradiating an electron ray perpendicularly to a sample and evaluating an atom and molecular arrangement using interference of a transparency electron or an elastic-scattering electron. It is possible to observe the array condition of a crystal lattice as plaid by using this technique. Therefore, the integrated state of the atoms in the grain boundary can be guessed by observing the grain boundary.

[0141] With the TEM photograph (drawing 19) which this invention persons acquired, the condition that two different crystal grain (cylindrical crystal grain) touched in the grain boundary was observed clearly. Moreover, it is checked by electron diffraction at this time that two crystal grain is outline {110} orientation although the gap of some is included in the crystallographic axis.

[0142] By the way, in the plaid observation by the above TEM photographs, the plaid corresponding to {111} sides was observed in {110} sides. In addition, the plaid corresponding to {111} sides has pointed out plaid to which {111} sides appear in a cross section, when crystal grain is cut along with the plaid. It can check in simple to what kind of field plaid corresponds with the distance between plaid.

[0143] As a result of observing in a detail the TEM photograph of the semi-conductor thin film obtained by the production approach of this example which these people mentioned above at this time, very interesting knowledge was acquired. In two different crystal grain which is visible to a photograph, the plaid corresponding to {111} sides was visible to both. And it was observed that mutual plaid is running in parallel clearly.

[0144] Furthermore, regardless of existence of the grain boundary, the plaid of two crystal grain which is different as crosses the grain boundary was connected. That is, although most plaid observed as crosses the grain boundary was the plaid of different crystal grain, it has checked continuing linearly. This was the same in the grain boundary of arbitration.

[0145] It is shown that two different crystal grain in the grain boundary has joined such the crystal structure (correctly structure of the grain boundary) with very sufficient adjustment. That is, in the grain boundary, a crystal lattice stands in a row continuously, and has composition which cannot make the trap level resulting from a crystal defect etc. very easily. If it puts in another way, it can be said that it is in a crystal lattice about a continuity in the grain boundary.

[0146] In addition, these people performed analysis by electron diffraction and HR-TEM observation to drawing 20 as a reference also about the conventional polycrystal silicon film (the so-called elevated-temperature polish recon film). Consequently, in two different crystal grain, mutual plaid is completely running scatteringly, and there was almost no junction which continues with sufficient adjustment in the grain boundary. That is, in the grain boundary, it became clear that there are many parts into which plaid broke off and there are many crystal defects.

[0147] this invention persons call adjustment association, a call, and the joint hand at that time an adjustment joint hand for the integrated state of an atom when plaid corresponds with sufficient adjustment like the semi-conductor thin film used for the liquid crystal panel of the semiconductor device of the invention in this application. Moreover, mismatching association, a call, and the joint hand at that time are called a mismatching joint hand (or azygos joint hand) for the integrated state of the atom in the case of seeing on the conventional polycrystal silicon film conversely mostly to which plaid does not correspond with sufficient adjustment like.

[0148] Since the adjustment in the grain boundary is extremely excellent, the semi-conductor thin film

used by the invention in this application has very few above-mentioned mismatching joint hands. As a result of this invention persons' investigating about two or more grain boundaries of arbitration, the abundance of a mismatching joint hand to the whole joint hand was 10% or less (preferably 5% or less, still more preferably 3% or less). That is, 90% or more (preferably 95% or more, still more preferably 97% or more) of the whole joint hand is constituted by the adjustment joint hand.
[0149] Moreover, the result of having observed the horizontal growth field produced according to the process of above-mentioned this example by electron diffraction is shown in drawing 21 (a). In addition, drawing 21 (b) is the electron diffraction pattern of the conventional polish recon film (what is called the elevated-temperature polish recon film) observed for the comparison.
[0150] The path of the exposure area of an electron ray is 4.25 micrometers, and the electron diffraction pattern shown in drawing 21 (a) and (b) has gathered the information on a field large enough. The photograph shown here is the typical diffraction pattern of a result which investigated two or more places of arbitration.
[0151] In the case of drawing 21 (a), the diffraction spot (diffraction mottle) corresponding to <110> incidence has appeared comparatively finely, and it can check that almost all crystal grain is carrying out {110} orientation in the exposure area of an electron ray. On the other hand, in the case of the conventional elevated-temperature polish recon film shown in drawing 21 (b), clear regularity was not looked at by the diffraction spot, but it became clear that the crystal grain of field bearings other than {110} sides was intermingled irregularly.
[0152] Thus, though it is the semi-conductor thin film which has the grain boundary, if an electron diffraction pattern is compared, the difference from the conventional semi-conductor thin film is clear [the point which shows the electron diffraction pattern which has regularity peculiar to {110} orientation is the description of the semi-conductor thin film used by the invention in this application, and].
[0153] As mentioned above, the semi-conductor thin film produced with the making process of this example shown in the above-mentioned was a semi-conductor thin film which has the crystal structure (correctly structure of the grain boundary) from which the conventional semi-conductor thin film completely differs. this invention persons are Japanese Patent Application No. 9-55633 about the result analyzed about the semi-conductor thin film used by the invention in this application. A number, 9-165216, and 9-212428 also explain.
[0154] Moreover, as an obstruction (barrier) with which the grain boundary of the semi-conductor thin film used by the above invention in this application checks migration of a carrier since 90% or more is constituted by the adjustment joint hand, there is almost no function. That is, it can be said that the semi-conductor thin film used by the invention in this application does not exist the grain boundary substantially.
[0155] Although functioned in the conventional semi-conductor thin film as an obstruction with which the grain boundary bars migration of a carrier, since such the grain boundary does not exist substantially, high carrier mobility is realized with the semi-conductor thin film used by the invention in this application. Therefore, the electrical property of TFT produced using the semi-conductor thin film used by the invention in this application shows the value which was very excellent. This thing is shown below.
[0156] [Knowledge about the electrical property of TFT]
[0157] Since it can consider substantially that the semi-conductor thin film used by the invention in this application is a single crystal (the grain boundary does not exist substantially), TFT which makes it a barrier layer shows the electrical property which is equal to MOSFET which used single crystal silicon. Data as shown below are obtained from TFT which this invention persons made as an experiment.
[0158] (1) The N channel mold TFT and the P channel mold TFT have a subthreshold level multiplier as small as 60 - 100 mV/decade (typically 60 - 85 mV/decade) used as the index of the switching engine performance (quick nature of a switch of ON / off actuation) of TFT.
(2) The electric field effect mobility (micro FE) used as the index of the working speed of TFT is as large as 100-300cm2/Vs (typically 150-200cm2/Vs) at the N channel mold TFT in 200-650cm2/Vs

(typically 250-300cm2/Vs) and the P channel mold TFT.
(3) The threshold electrical potential difference (Vth) used as the index of the driver voltage of TFT is as small as -1.5-0.5 V in -0.5-1.5 V and the P channel mold TFT at the N channel mold TFT.
[0159] As mentioned above, it is checked that the switching characteristic and the high-speed operation property of having excelled extremely can be realized.
[0160] In addition, the annealing process in the temperature beyond the crystallization temperature which was mentioned above in forming CGS (700-1100 degrees C) has played the important role about the defective reduction in crystal grain. That is explained below.
[0161] Drawing 22 (a) is the TEM photograph which expanded the crystal silicone film in the time of ending even the above-mentioned crystallization process by 250,000 times, and the defect which is in sight on zigzag as shown by the arrow head in crystal grain (a black part and a white part originate in the difference of contrast, and appear) is checked.
[0162] Although it is the stacking fault which the pile sequence of the atom of a silicon crystal plane mainly contradicts as such a defect, there are also cases, such as a rearrangement. Drawing 22 (a) is considered to be the stacking fault which has a defective side parallel to {111} sides. That can be checked also from the defect which is in sight in the shape of zigzag having made the include angle which is about 70 degrees, and having bent.
[0163] On the other hand, as shown in drawing 22 (b), in crystal grain, the defect which originates at a stacking fault, a rearrangement, etc. is hardly seen, but the crystal silicone film used for this invention seen for this scale factor can check that crystallinity is very high. This inclination is being able to say about the whole film surface, and although it is difficult in the present condition to make the number of defects into zero, it can decrease even to extent it can be considered substantially that is zero.
[0164] That is, since the defect in crystal grain is reduced by even extent which can almost be disregarded and the grain boundary cannot become the obstruction of carrier migration with a high continuity, it can be considered on a single crystal or a real target that the crystal silicone film used for the liquid crystal panel of the semiconductor device of this invention is a single crystal.
[0165] Thus, although both crystal silicone films which drawing 22 (a) and a photograph with (b) showed have the almost equivalent continuity in the grain boundary, there is a big difference in the number of defects in crystal grain. The reason which shows an electrical property with the crystal silicone film far more expensive than the crystal silicone film shown in drawing 22 R> 2 (a) shown in drawing 22 (b) has a large place by the difference of this number of defects.
[0166] In producing CGS, the above thing shows that the gettering process of a catalyst element is an indispensable process. this invention persons consider the following models about the phenomenon which happens according to this process.
[0167] First, in the condition which shows in drawing 22 (a), the catalyst element (typically nickel) is segregating to the defect in crystal grain (mainly stacking fault). That is, it is thought that much association of the form of Si-nickel-Si exists.
[0168] However, it is Si-nickel when nickel which exists in a defect by performing the gettering process of a catalyst element is removed. Association goes out. Therefore, the joint hand in which silicon remained is Si-Si immediately. Association is formed and it is stabilized. In this way, a defect is extinguished.
[0169] Of course, although it is known that the defect in a crystal silicone film will be extinguished by heat annealing in high temperature, association with nickel goes out and it can be surmised that recombination of silicon for many uncombined hands to occur is performed smoothly.
[0170] Moreover, between a crystal silicone film and its substrate fixed this invention persons by heat-treating at the temperature beyond crystallization temperature (700-1100 degrees C), and the model that a defect is extinguished because adhesion increases is also considered.
[0171] in this way, the crystal silicone film (as compared with drawing 22 (a), it is markedly alike, and has the description that few defects in crystal grain are.) with which the obtained crystal silicone film (drawing 22 (b)) only crystallized By electron-spin-resonance analysis (Electron Spin Resonance:ESR), the difference of this number of defects turns into a difference of spin density, and appears. The spin

density of the crystal silicone film used for this invention in the present condition is 3 at least 1x1018 pieces/cm. It is the following (it is 3 5x1017 pieces/cm typically following).
[0172] The crystal silicone film used for this invention which has the above crystal structures and descriptions is called continuous grain boundary crystal silicon (Continuous Grain Silicon:CGS).
[0173] (Example 3)
[0174] In this example, the semi-conductor display which has the drive circuit stated in the example 1 is produced with a reverse stagger mold.
[0175] Drawing 11 is referred to. The sectional view of the active-matrix substrate of the semi-conductor indicating equipment of this example is shown in drawing 11 . In addition, the CMOS circuit is shown as a typical circuit of the drive circuit of a semi-conductor display by a diagram. Moreover, the pixel matrix circuit and the other circumference circuits which are constituted by Pixel TFT are also formed in coincidence.
[0176] 1101 -- a substrate and 1102 -- a substrate insulator layer, and 1103 and 1104 -- a gate electrode and 1105 -- gate dielectric film, and 1106 and 1107 -- the source drain field of N type TFT, and 1108 and 1109 -- a low concentration impurity range and 1110 -- for a low concentration impurity range and 1115, as for a channel stopper and 1118, an interlayer insulation film, and 1119, 1120 and 1121 are [a channel formation field, and 1116 and 1117 / the source drain field of P type TFT, and 1113 and 1114 / a channel formation field, and 1111 and 1112] source drain electrodes. In addition, channel stoppers 1116 and 1117 function as a doping mask at the time of producing the channel formation field of N type or P type TFT.
[0177] The semi-conductor barrier layer of this example may be polycrystal-ized by the approach of an example 2.
[0178] Moreover, the semi-conductor barrier layer of this example may be polycrystal-ized using a laser annealing technique.
[0179] Moreover, an example 2 shall be followed about other configurations.
[0180] (Example 4)
[0181] In this example, the semi-conductor display which has the drive circuit stated in the example 1 is produced with a different reverse stagger mold from what was stated in the example 3.
[0182] Drawing 12 is referred to. For gate dielectric film, and 1206 and 1207, a semi-conductor barrier layer, and 1208 and 1209 are [a substrate insulator layer and 1203 and 1204 / 1201 / a substrate and 1202 / a gate electrode and 1205] n+. A layer, and 1210 and 1211 are p+. As for a layer, and 1212, 1213 and 1214, a source drain electrode and 1215 are channel protective coats.
[0183] The semi-conductor barrier layer of this example may be polycrystal-ized by the approach of an example 2.
[0184] Moreover, the semi-conductor barrier layer of this example may be polycrystal-ized using a laser annealing technique.
[0185] Moreover, an example 2 shall be followed about other configurations.
[0186] (Example 5)
[0187] This example explains an example of the concrete circuitry of a switching circuit. In this example, the block diagram of the main **** of a active-matrix mold semi-conductor indicating equipment will be shown. An example 1 can be referred to about a shift register circuit and a latch circuit. In addition, also in this example, the active matrix liquid crystal display which used liquid crystal for the display medium can be constituted.
[0188] Drawing 15 is referred to. The block diagram of the principal part of the active-matrix mold semi-conductor indicating equipment of this example is shown in drawing 15 . As for a different point from an example 1, that the source signal-line side drive circuit is used up and down across a pixel matrix circuit, that the gate signal line side drive circuit is used for right and left across a pixel matrix circuit, the level-shifter circuit's being used for the source signal-line side drive circuit, and a digital video-data dividing network may be prepared. Moreover, although a D/A conversion circuit like an example 1 can also be used about a D/A conversion circuit, a digital video data can be divided into a high order bit and a lower bit, and analog video-signal-ization of a digital video data can also be carried

out by the 1st and 2nd D/A conversion circuits. Moreover, it is not necessary to necessarily use a level-shifter circuit that what is necessary is just to use if needed.

[0189] The active matrix liquid crystal display of this example has the source signal-line side drive circuit A1501, the source signal-line side drive circuit A1502, the gate signal line side drive circuit A1512, the source signal-line side drive circuit A1515, the pixel matrix circuit 1516, and the digital video-data dividing network 1510.

[0190] The source signal-line side drive circuit A1501 is equipped with a shift register circuit 1502, a buffer circuit 1502, latch circuit (1) 1504, latch circuit (2) 1505, selector (switch) circuit (1) 1508, the level-shifter circuit 1507, the D/A conversion circuit 1508, and selector (switch) circuit (2) 1509. The source signal-line side drive circuit A101 supplies a video signal (gradation voltage signal) to the odd-numbered source signal line. In addition, in this example, the circuit equivalent to the switching circuit explained in the above-mentioned example 1 will be called a selector circuit.

[0191] Actuation of the source signal-line side drive circuit A1501 is explained. A start pulse and a clock signal are inputted into a shift register circuit 1501. A shift register circuit 1501 carries out sequential supply of the timing signal in a buffer circuit 1503 based on an above-mentioned start pulse and an above-mentioned clock signal.

[0192] The buffer of the timing signal from a shift register circuit 1502 is carried out by the buffer circuit 1503. Since many circuits or components are connected even to the source signal line connected to the pixel matrix circuit 1518 from the shift register circuit 1502, load-carrying capacity is large. " of the timing signal produced since this load-carrying capacity is large -- in order to become blunt and to prevent ", this buffer circuit 103 is formed.

[0193] The timing signal by which the buffer was carried out in the buffer circuit 1503 is supplied to latch circuit (1) 1504. Latch circuit (1) 1504 contains 960 latch circuits treating 2-bit data. Latch circuit (1) If said timing signal is inputted, 1504 will incorporate the digital signal supplied from a digital video-data dividing network one by one, and will hold it.

[0194] Latch circuit (1) Time amount until the writing of a digital signal to all the latch circuits of 1504 is completed briefly is called an one-line period (horizontal scanning period). That is, the time interval of the time of the writing of the digital video data from the time of the writing of the digital video data from a digital video-data dividing network being started to the latch circuit of most left-hand side in latch circuit (1) 1504 to the latch circuit of most right-hand side being completed is an one-line period.

[0195] Latch circuit (1) After the writing of the digital video data to 1504 is completed, when a latch pulse flows according to the timing of a shift register circuit 1502 of operation on the latch pulse line connected to latch circuit (2) 1505, the digital video datas written in latch circuit (1) 1504 are sent out to latch circuit (2) 1505 all at once, and are written in them.

[0196] The writing of the digital video data again supplied from a digital video-data dividing network is performed one by one in latch circuit (1) 1504 which finished sending out a digital video data to latch circuit (2) 1505 by the timing signal from a shift register circuit 1502. Especially actuation of such a latch circuit (1) and a latch circuit (2) does not differ from an example 1.

[0197] During the one-line period of eye this 2 order, sequential selection of the digital video data sent out to the latch circuit (2) to compensate for initiation of the one-line period of eye 2 order is made by selector circuit (1) 1506. About the configuration and actuation of the selector circuit of this example, it mentions later.

[0198] Selector circuit (1) A 2-bit digital video data is supplied to a level shifter 1507 from the latch circuit chosen by 1506. The voltage level of a digital video data is raised by the level shifter 1507, and is supplied to the D/A conversion circuit 1508. The D/A conversion circuit 1508 changes a 2-bit digital video data into an analog signal (gradation electrical potential difference), and sequential supply is carried out at the source signal line chosen by selector circuit (2) 1509. The analog signal supplied to a source signal line is supplied to the source field of the pixel TFT of the pixel matrix circuit connected to the source signal line.

[0199] In the gate signal line side drive circuit A1512, the timing signal from a shift register 1513 is supplied to a buffer circuit 1514, and is supplied to a corresponding gate signal line (scanning line).

Since the gate electrode of the pixel TFT for one line is connected to the gate signal line and all the pixels TFT must be turned ON by one line at coincidence, what has big current capacity is used for a buffer circuit 1514.

[0200] Thus, switching of TFT which corresponds with the scan signal from a gate signal line side shift register is performed, the analog signal (gradation electrical potential difference) from a source signal-line side drive circuit is supplied to Pixel TFT, and a liquid crystal molecule drives.

[0201] 1511 is the source signal-line side drive circuit B, and the configuration is the same as the source signal-line side drive circuit A1501. The source signal-line side drive circuit B1511 supplies a video signal to the even-numbered source signal line.

[0202] 1515 is the gate signal line side drive circuit B, and takes the same configuration as the gate signal line side drive circuit A1512. In this example, by establishing a gate signal line side drive circuit in the both ends of the pixel matrix circuit 1516 in this way, and operating both gate signal line side drive circuits, also when one of the two does not operate, a poor display is not caused.

[0203] 1510 is a digital video-data dividing network. The digital video-data dividing network 1510 is a circuit for dropping on 1/m the frequency of the digital video data inputted from the outside. By dividing a digital video data, the frequency of a signal required for actuation of a drive circuit can also be dropped on 1/m.

[0204] In addition, it is indicated by Japanese Patent Application No. No. 356238 [nine to] that whose a digital video-data dividing network is really formed on the same substrate as a pixel matrix circuit or other drive circuits it is the patent application by these people. Explanation of actuation of a digital video-data dividing network should be made by said patent application at the detail, and when you understand actuation of the digital video-data dividing network of this example, please make it reference.

[0205] The pixel matrix circuit 116 takes the configuration by which the pixel TFT of the width 1920x length 1080 has been arranged in the shape of a matrix.

[0206] When only the number of the scanning lines repeats the actuation mentioned above, one screen (one frame) is formed. In the active matrix liquid crystal display of this example, rewriting of the image of 60 frames is performed in 1 second.

[0207] Here, the configuration and actuation of selector circuit (1) 1506 of this example and selector circuit (2) 1509 are explained. The fundamental concept of a selector circuit is the same as the switching circuit explained in the example 1. In this example, one a selector circuit (1) and a selector circuit (2) are used for every four source signal lines. Therefore, 240 selector circuits (1) and 240 selector circuits (2) are used for the source signal-line side drive circuit (A), and 240 selector circuits (1) and 240 selector circuits (2) are used for the source signal-line side drive circuit (B).

[0208] Drawing 16 is referred to. The selector circuit (1) of the leftmost of the expedient top of explanation and a source signal-line side drive circuit (A) is shown in drawing 16 . These 240 selector circuits are used for the actual source signal-line side drive circuit.

[0209] One of the selector circuits (1) of this example has eight 3 input NAND circuits, two 4 input NAND circuits, and two inverters, as shown in drawing 16 . In selector circuit (1) 1506 of this example the signal from latch circuit (2) 1505 inputs -- having -- the signal line L0 from latch circuit (2) 1505, 0, and L -- 0, 1, L1, 0, L1, 1, and ... A signal line L0, 0, L0, 1, L1, 0, L1, 1, L2, 0, L2, 1, L3, 0, L3, and 1 are connected to the selector circuit (1) shown in drawing 16 among L1919, 0, L1919, and 1. The publication La and b means that the bit [b-th] signal of the digital video data supplied to the a-th source signal line from the left is supplied. Moreover, a timing signal is inputted into a selector circuit (1) from signal lines SS1 and SS2. The signal from a selector circuit (1) is inputted into a level shifter 1507, and is inputted into the D/A conversion circuit 1508 after that.

[0210] Here, drawing 17 is referred to. The selector circuit (2) is shown in drawing 17 . The leftmost expedient top selector circuit (2) of explanation is shown in drawing 17 . These 240 selector circuits are used for the actual source signal-line side drive circuit.

[0211] The selector circuit (2) of this example has four analog switches which have three P channel molds TFT and three N channel molds TFT, and three inverters, as shown in drawing 17 . The analog

video signal changed into the analog signal by the D/A conversion circuit 1508 is inputted into a selector circuit (2).

[0212] The timing chart of the 2-bit data inputted into selector circuit (1) 1506 and selector circuit (2) 1509 and a timing signal is shown in drawing 18 . LS is a latch signal and is a signal supplied to a latch circuit (2) at the time of initiation of an one-line period (horizontal scanning period). bit-0 and bit-1 show the data (the 0th bit of the digital picture signal outputted from a latch circuit (2), and 1st bit), respectively. To the signal line L0 from a latch circuit (2) connected to the selector circuit (1) shown in drawing 16 here, 1 and L0, and 0, in addition, respectively The digital signal of A1 and A0 is supplied. To a signal line L1, 1 and L1, and 0, respectively The digital signal of B1 and B0 is supplied, and the digital signal of C1 and C0 is supplied to a signal line L2, 1 and L2, and 0, respectively, and suppose a signal line L3, 1 and L3, and 0 that the digital signal of D1 and D0 is supplied, respectively.

[0213] In a selector circuit (1), the signal outputted to bit-1 and bit-0 is chosen based on the timing signal supplied to SS1 and SS2. That is, A1 is outputted to bit-1 at the first Rhine (1/4) period, and A0 is outputted to bit-0. B1 is outputted to bit-1 at the next Rhine (1/4) period, and B0 is outputted to bit-0. C1 is outputted to bit-1 at the next Rhine (1/4) period, and C0 is outputted to bit-0. And D1 is outputted to bit-1 at the last Rhine (1/4) period, and D0 is outputted to bit-0. Thus, the data from the Rhine (1/4) period [every] latch circuit (2) will be supplied to a level-shifter circuit.

[0214] In addition, the D/A conversion circuit indicated by Japanese Patent Application No. No. 344351 [nine to] and Japanese Patent Application No. No. 365054 [nine to] which are these people's patent application as an example of the D/A conversion circuit which can be used for the D/A conversion circuit 1508 can be raised. As mentioned above, the D/A conversion circuit currently indicated by such patent application divided the digital video data into the high order bit and the lower bit, and has made the analog video signal by using two D/A conversion circuits. For example, when using a 4-bit digital video data, it may divide into 2 bits of high orders, and 2 bits of low order, and D/A conversion may be performed.

[0215] The analog video signal supplied from a D/A conversion circuit is chosen by the selector circuit (2), and is supplied to a source signal line. Although an analog video signal is supplied to the source signal line which corresponds the Rhine (1/4) period every also in this case, only while the electrical potential difference of an analog signal is completely decided with the decoding enable signal (DE), an analog video signal will be supplied to a source signal line.

[0216] In addition, in this example, although the 2-bit digital video data was treated, a digital video data 2 bits or more can also be treated.

[0217] Moreover, although the number of D/A conversion circuits was made into the conventional quadrant in this example using the switching circuit in order to prepare a 1 D/A conversion circuit in four source signal lines, this invention can also make the number of D/A conversion circuits numbers other than this. For example, when one D/A conversion circuit per eight source signal lines is assigned, in the semi-conductor display of this example, the number of D/A conversion circuits becomes 240 pieces, and the further reductions of area of a drive circuit are realized. Thus, it is not limited to this example whether one D/A conversion circuit per how many source signal lines is assigned.

[0218] therefore, when the semi-conductor display of this invention has m source signal lines (m is the natural number) (if it puts in another way -- the number of pixels (horizontal x length) -- mx -- arbitrary cases), as one line, m x bit digital gradation signals (x is the natural number) are supplied. in this case -- if the semi-conductor display of this invention considers as D/A conversion circuit section preparation ****** which has n D/A conversion circuits (n is the natural number) -- every -- D / A conversion circuit will carry out analogue conversion of the digital gradation signal of a m/n individual one by one, and will carry out sequential supply of the analog signal to the source line of a corresponding m/n book. In addition, what is necessary is just to use the D/A conversion circuit according to the number of bits of a digital gradation signal.

[0219] Since the number of the D/A conversion circuits which occupy a big area also in a drive circuit can be made into the conventional quadrant according to this example, even if it takes the increment for a selector circuit into consideration, the miniaturization of a semi-conductor display is realizable.

[0220] (Example 6)
[0221] Moreover, although the above-mentioned examples 2-5 have explained the liquid crystal panel of a transparency mold, it cannot be overemphasized that the drive circuit of an example 1 is used also for the liquid crystal panel of a reflective mold. Moreover, a ferroelectric liquid crystal, antiferroelectricity liquid crystal, etc. can also be used for a liquid crystal ingredient.
[0222] Moreover, although intermediary explanation has been given in the above-mentioned examples 2-5 when using liquid crystal as a display medium, the drive circuit of an example 1 can be used also for the mixolimnion of liquid crystal and a macromolecule, and the so-called polymer dispersed liquid crystal display. Moreover, the drive circuit of an example 1 may answer applied voltage, and may be used for the display which has what kind of display medium of others by which an optical property may be modulated. For example, electroluminescence devices, an erection potter's wheel mix component, etc. may be used as a display medium.
[0223] (Example 7)
[0224] There are ** and various applications about the semi-conductor display of the above-mentioned examples 1-6. This example explains the semiconductor device incorporating the semi-conductor display of this invention.
[0225] A video camera, a still camera, a projector, a head mount display, car navigation, a personal computer, Personal Digital Assistants (a mobile computer, cellular phone, etc.), etc. are mentioned to such a semiconductor device. Those examples are shown in drawing 13 .
[0226] Drawing 13 (A) is a cellular phone and consists of a body 1301, the voice output section 1302, the voice input section 1303, a semi-conductor indicating equipment 1304, an actuation switch 1305, and an antenna 1306.
[0227] Drawing 13 (B) is a video camera and consists of a body 1401, the semi-conductor indicating equipment 1402, the voice input section 1403, an actuation switch 1404, a dc-battery 1405, and the television section 1406.
[0228] Drawing 13 (C) is a mobile computer and consists of a body 1501, the camera section 1502, the television section 1503, an actuation switch 1504, and a semi-conductor display 1505.
[0229] Drawing 13 (D) is a head mount display, and consists of a body 1601, a semi-conductor indicating equipment 1602, and the band section 1603.
[0230] Drawing 13 (E) is a rear mold projector, and, as for a polarization beam splitter, and 1705 and 1706, for the light source and 1703, a semi-conductor indicating equipment and 1704 are [1701 / a body and 1702 / a reflector and 1707] screens. In addition, as for a rear mold projector, it is desirable that the include angle of a screen can be changed with the location which a viewer looks at, with a body fixed.
[0231] Drawing 13 (F) is a front mold projector, and consists of a body 1801, the light source 1802, a semi-conductor display 1803, optical system 1804, and a screen 1805.
[0232]
[Effect of the Invention]
[0233] Since the semi-conductor display of this invention can lessen sharply conventionally the number of the D/A conversion circuits which occupy a big area also in the drive circuit, it can realize the miniaturization of a semi-conductor display.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the schematic diagram of the semi-conductor display of the conventional digital gradation.
[Drawing 2] It is the schematic diagram of the semi-conductor display by the operation gestalt with this invention.
[Drawing 3] It is the timing chart of the source signal line of the semi-conductor indicating equipment by the operation gestalt with this invention.
[Drawing 4] It is the block diagram of the D/A transducer by the operation gestalt with this invention.
[Drawing 5] It is the timing chart of the D/A transducer by the operation gestalt with this invention.
[Drawing 6] It is drawing showing the making process of the semi-conductor display by the operation gestalt with this invention.
[Drawing 7] It is drawing showing the making process of the semi-conductor display by the operation gestalt with this invention.
[Drawing 8] It is drawing showing the making process of the semi-conductor display by the operation gestalt with this invention.
[Drawing 9] It is the sectional view of the semi-conductor display by the operation gestalt with this invention.
[Drawing 10] It is the plan and side elevation of a semi-conductor display by the operation gestalt with this invention.
[Drawing 11] It is the sectional view of the active-matrix substrate of the semi-conductor indicating equipment by the operation gestalt with this invention.
[Drawing 12] It is the sectional view of the active-matrix substrate of the semi-conductor indicating equipment by the operation gestalt with this invention.
[Drawing 13] It is the example of the semiconductor device carrying the semi-conductor display of this invention.
[Drawing 14] It is the partial block diagram of the semi-conductor display by the embodiment with this invention.
[Drawing 15] It is the block diagram of the semi-conductor indicating equipment by the operation gestalt with this invention.
[Drawing 16] It is the circuitry Fig. of the selector circuit (switching circuit) by the operation gestalt with this invention.
[Drawing 17] It is the circuitry Fig. of the selector circuit (switching circuit) by the operation gestalt with this invention.
[Drawing 18] It is the timing chart of the selector circuit by the operation gestalt with this invention.
[Drawing 19] It is the photograph Fig. of the semi-conductor display by the operation gestalt with this invention.
[Drawing 20] It is the TEM photograph Fig. of CGS.
[Drawing 21] It is the TEM photograph Fig. of elevated-temperature polish recon.

[Drawing 22] It is the photograph Fig. showing the electron diffraction pattern of CGS and elevated-temperature polish recon.
[Drawing 23] It is the TEM photograph Fig. of CGS and elevated-temperature polish recon.
[Description of Notations]
201 Source Signal-Line Side Shift Register
202 Digital Decoder
203 Latch Circuit
204 Latch Circuit
205 Signal Line
206 Signal Line
207 D/A Conversion Circuit Section
208 D/A Conversion Circuit
209 Switching Circuit
210 Switching Circuit
211 Source Signal Line
212 Gate Signal Line Side Shift Register
213 Gate Signal Line
214 Pixel TFT

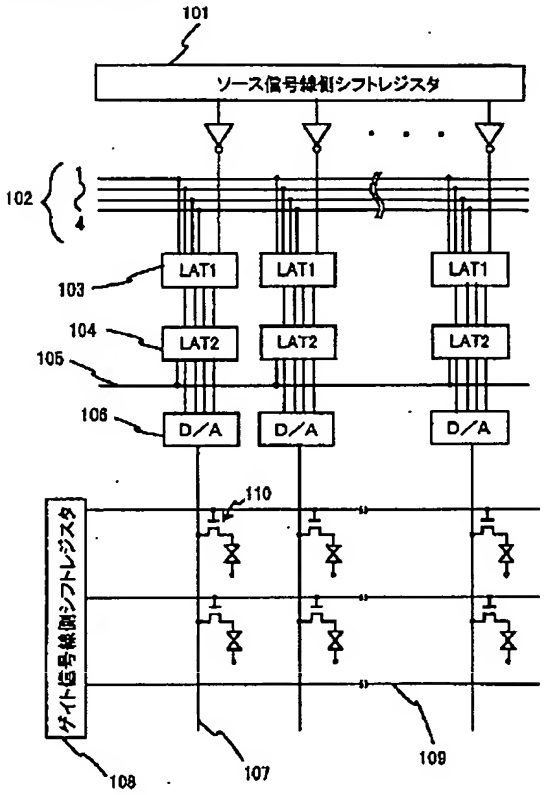
[Translation done.]

* NOTICES *

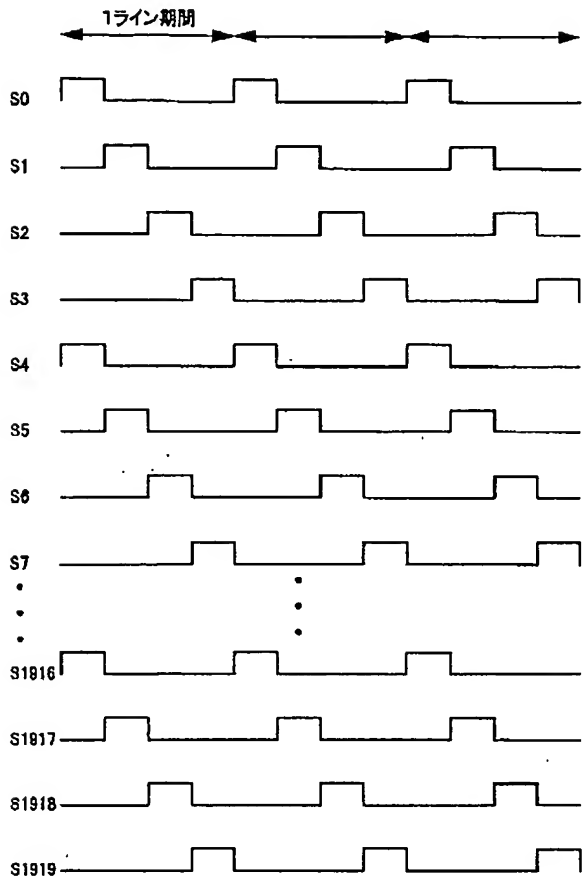
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

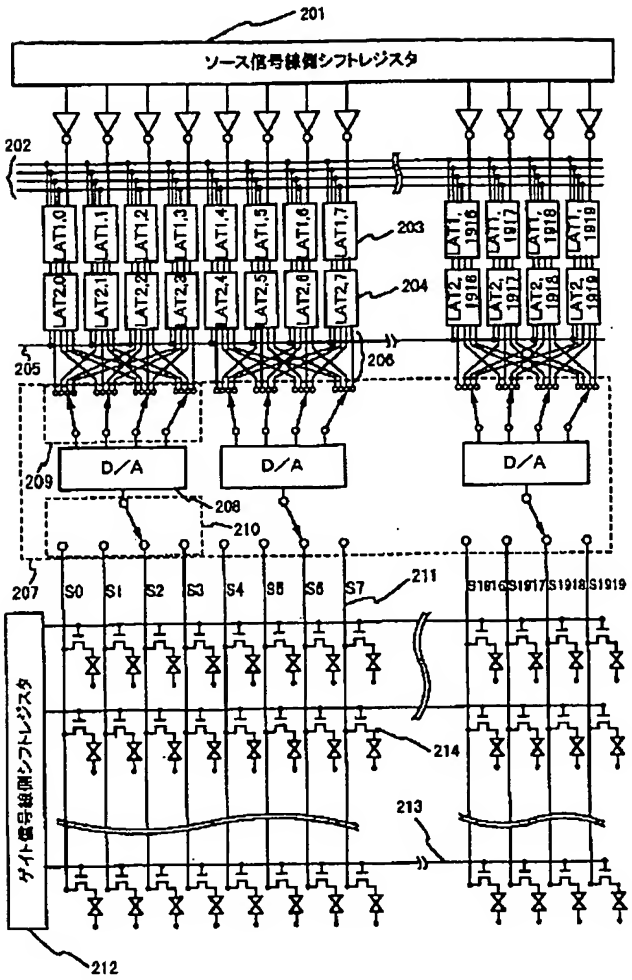
[Drawing 1]



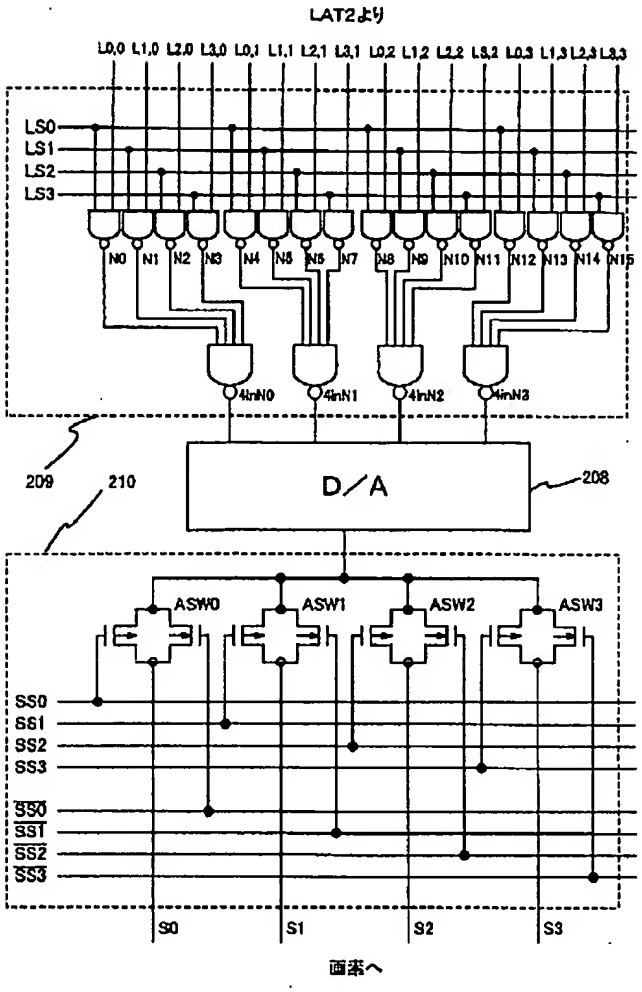
[Drawing 3]



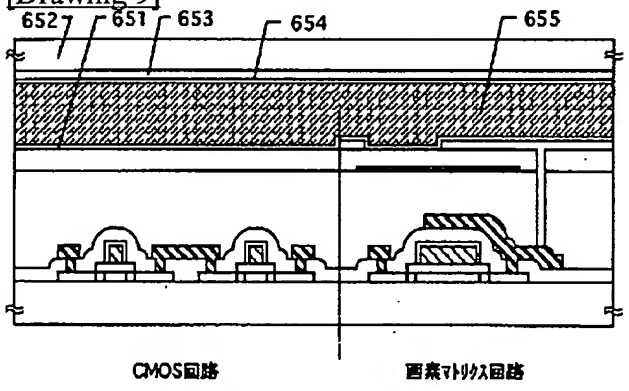
[Drawing 2]


201
ソース信号線側シフトレジスタ
202
203
204
205
206
D/A
D/A
D/A
209
208
210
207
S0
S1
S2
S3
S4
S5
S6
S7
211
S1916
S1917
S1918
S1919
214
213
ゲート信号線側シフトレジスタ
212

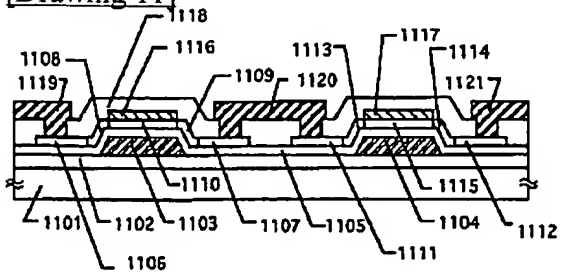
[Drawing 4]



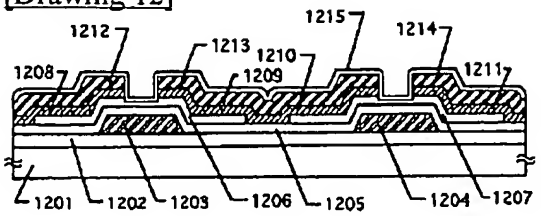
[Drawing 9]



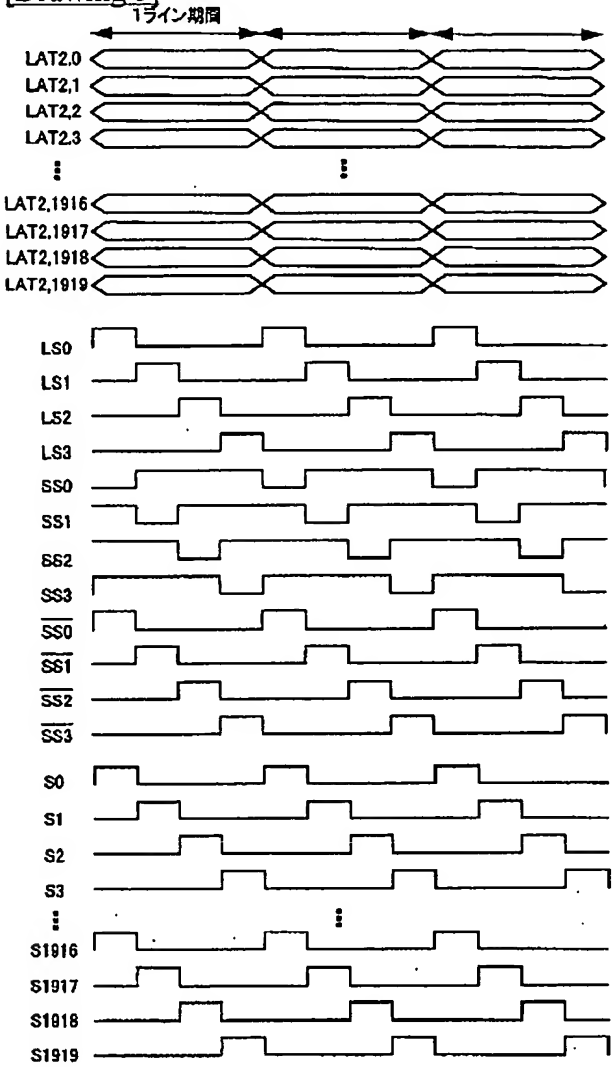
[Drawing 11]



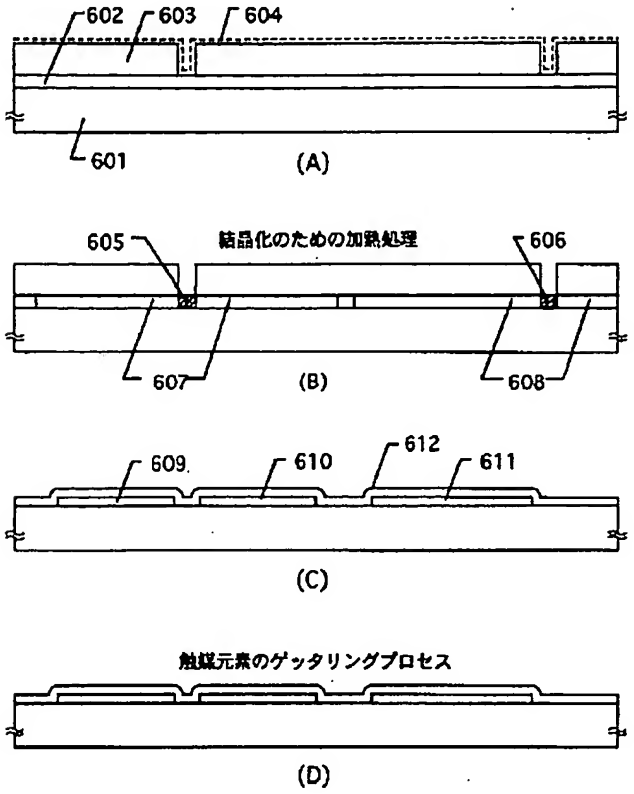
[Drawing 12]



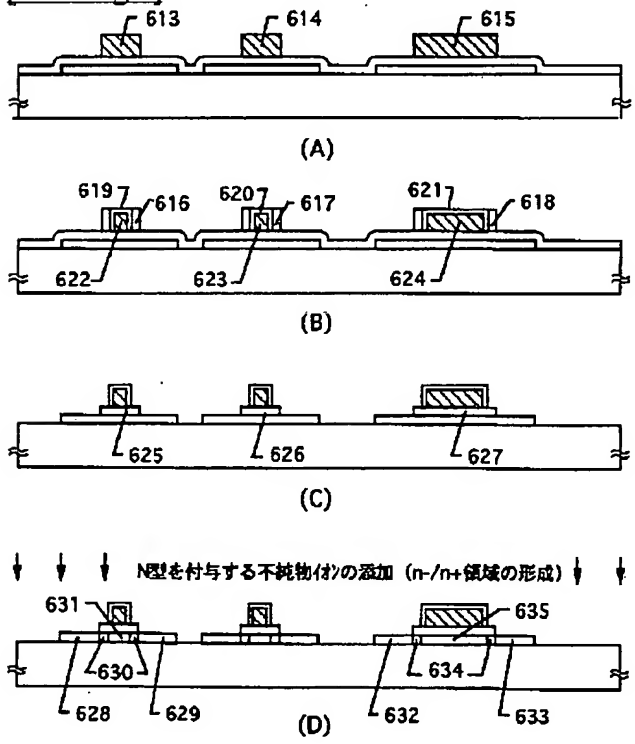
[Drawing 5]



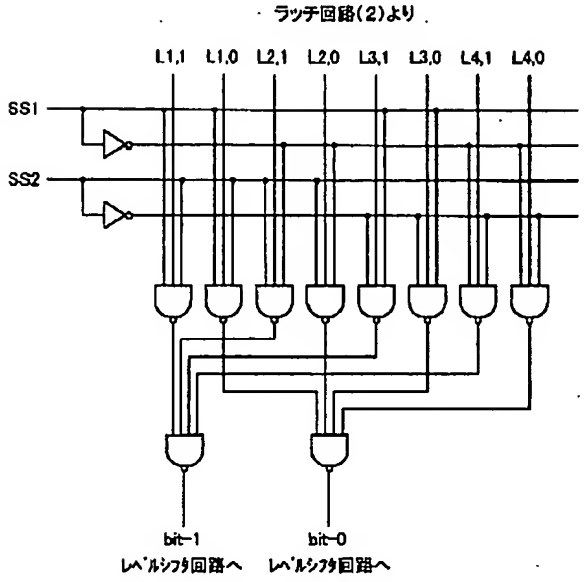
[Drawing 6]



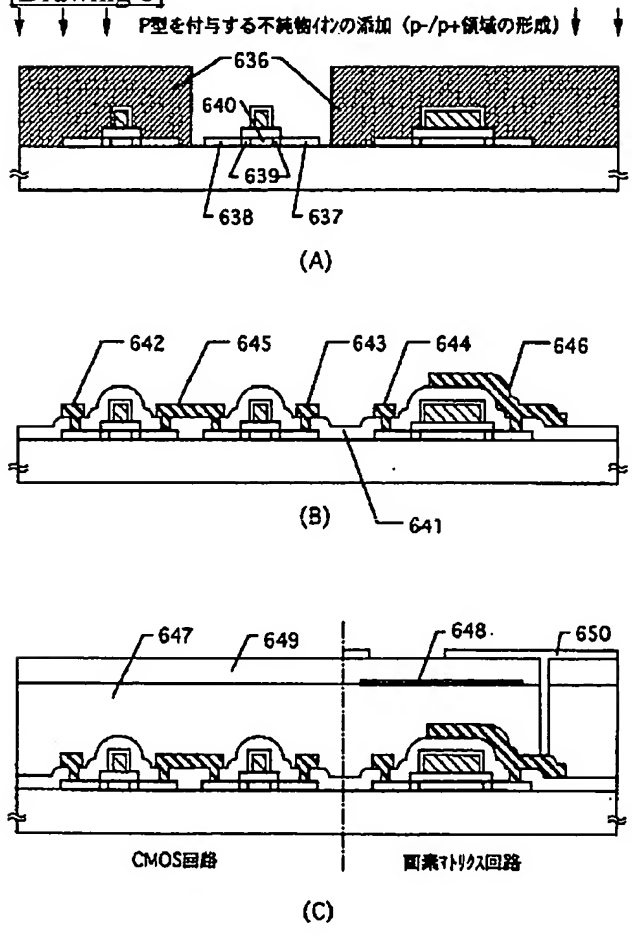
[Drawing 7]



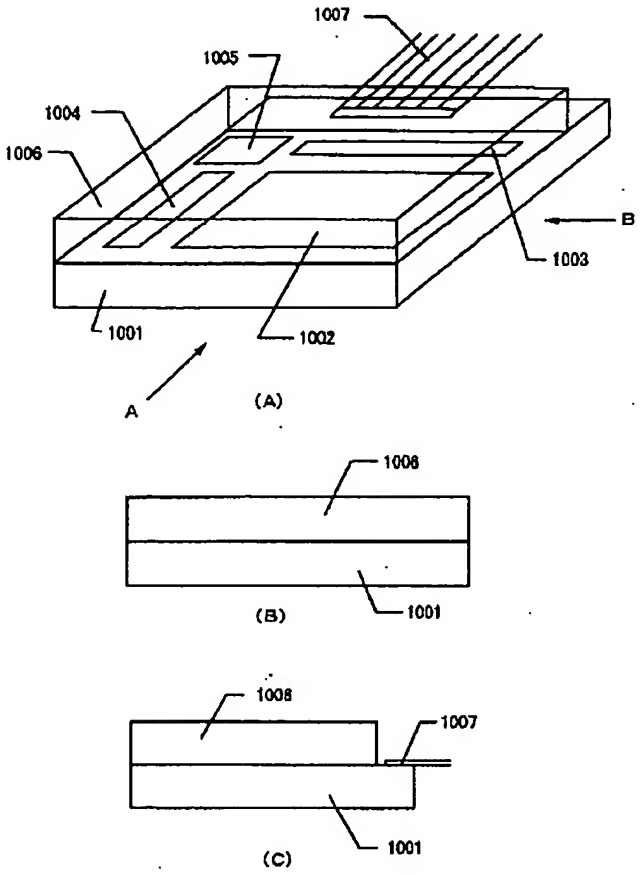
[Drawing 16]



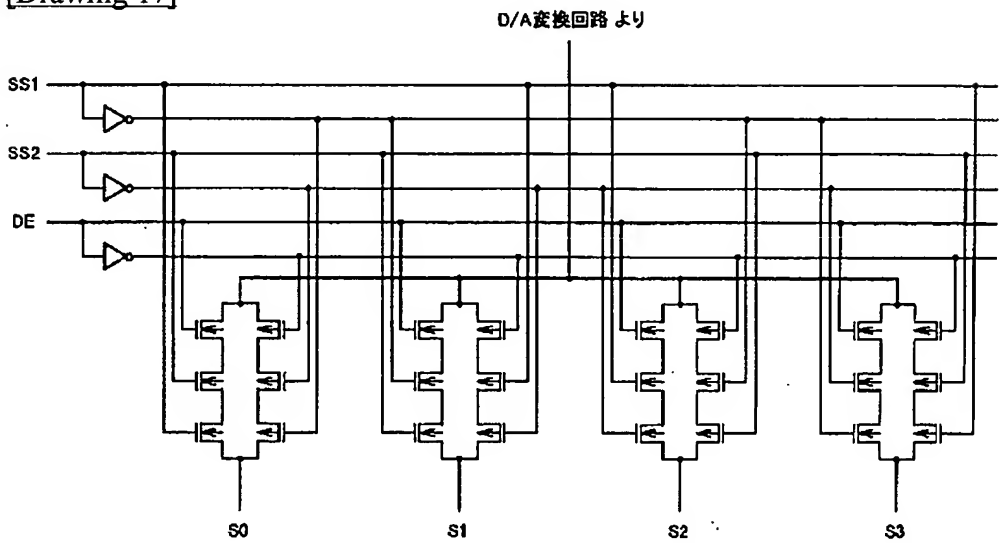
[Drawing 8]



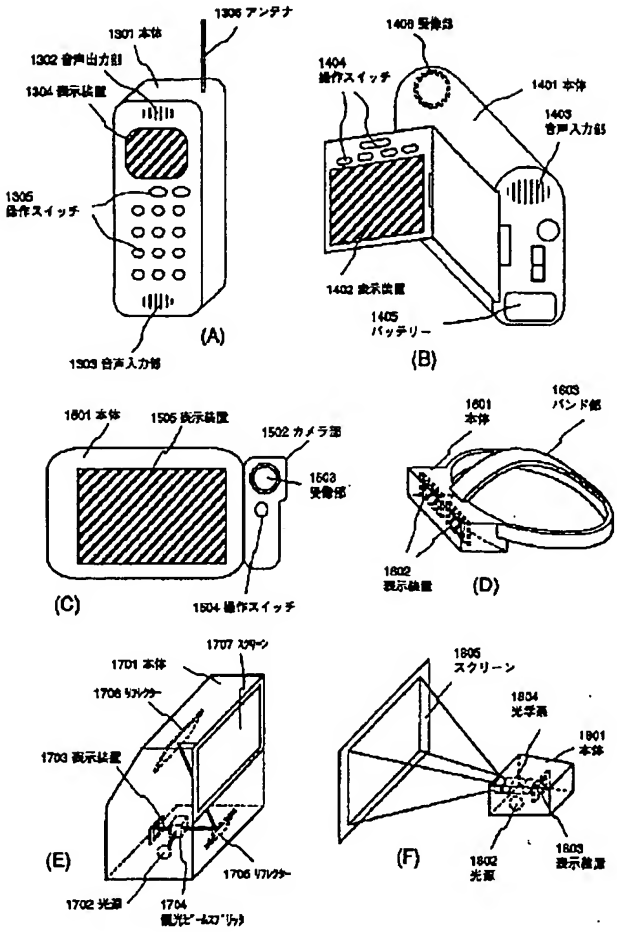
[Drawing 10]



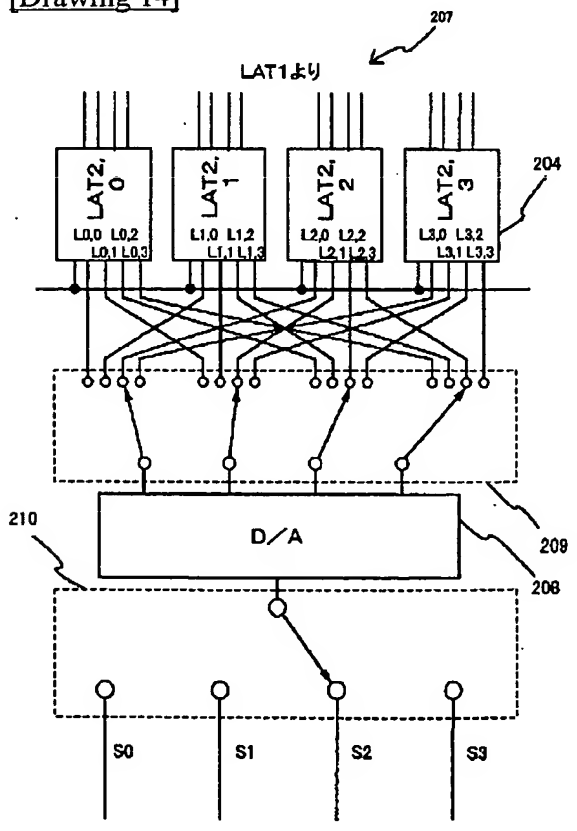
[Drawing 17]



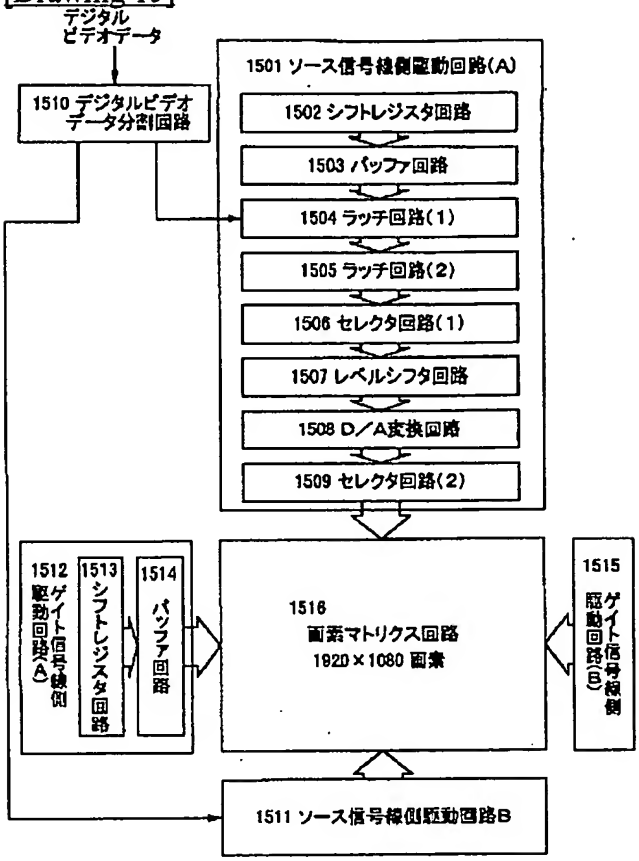
[Drawing 13]


1306 アンテナ
1301 本体
1302 音声出力部
1304 表示装置
1305 操作スイッチ
1303 音声入力部
(A)
1406 受像部
1404 操作スイッチ
1401 本体
1403 音声入力部
1402 表示装置
1405 バッテリー
(B)
1501 本体
1505 表示装置
1502 カメラ部
1503 受像部
1504 操作スイッチ
(C)
1601 本体
1603 バンド部
1602 表示装置
(D)
1701 本体
1707 スクリーン
1708 リフレクター
1703 表示装置
1702 光源
1704
1706 リフレクター
(E)
1805 スクリーン
1804 光学系
1801 本体
1802 光源
1803 表示装置
(F)

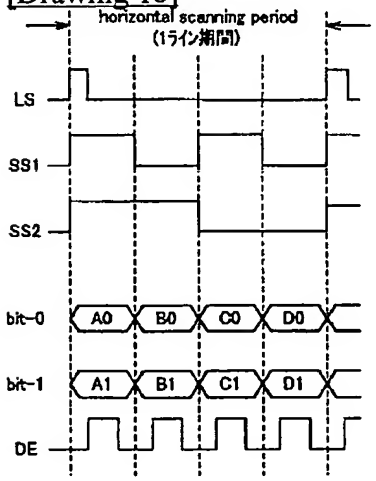
[Drawing 14]


207
LAT1より
LAT2, 0
LAT2, 1
LAT2, 2
LAT2, 3
L0,0 L0,2
L0,1 L0,3
L1,0 L1,2
L1,1 L1,3
L2,0 L2,2
L2,1 L2,3
L3,0 L3,2
L3,1 L3,3
204
210
D/A
209
208
S0
S1
S2
S3

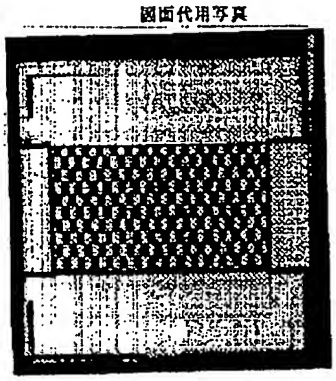
[Drawing 15]



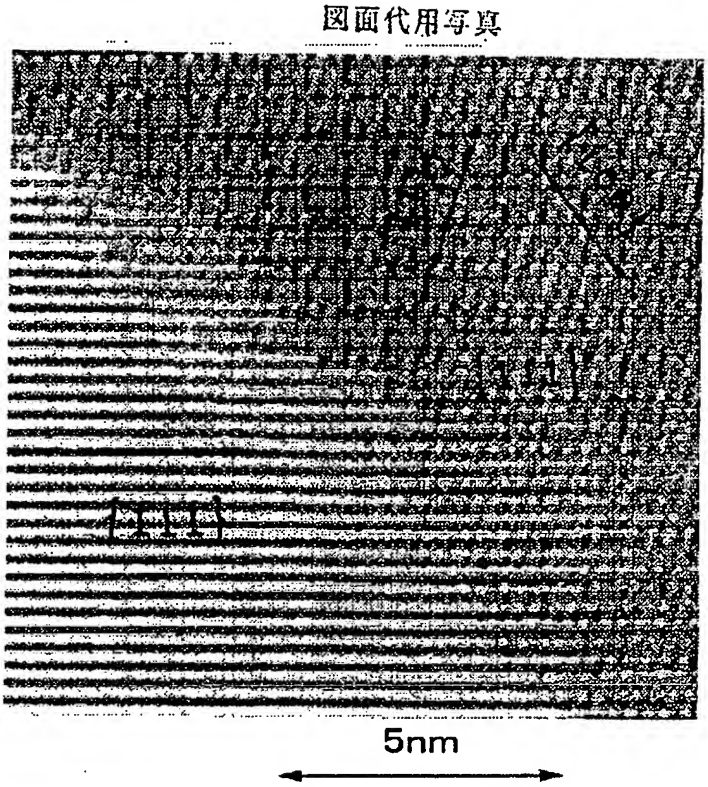
[Drawing 18]



[Drawing 19]

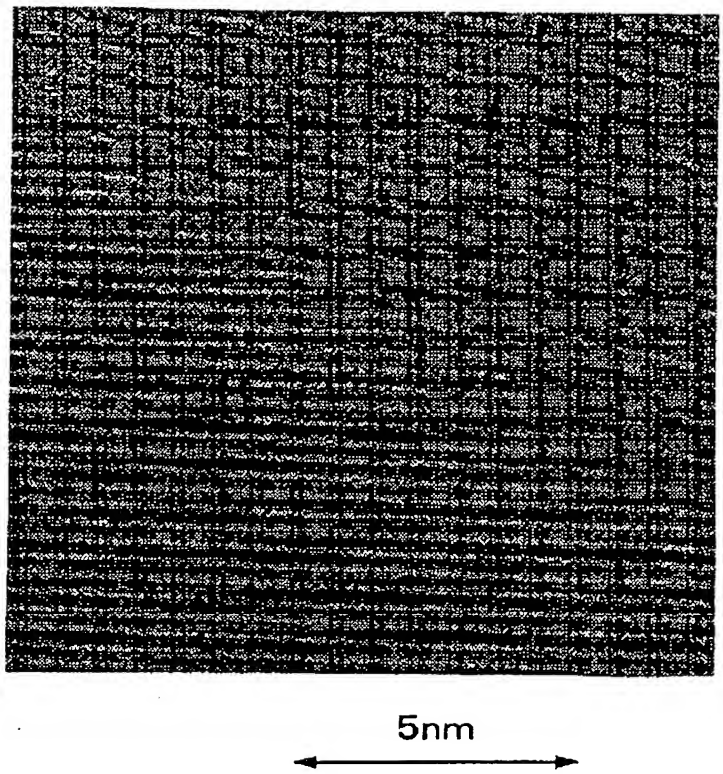


[Drawing 20]



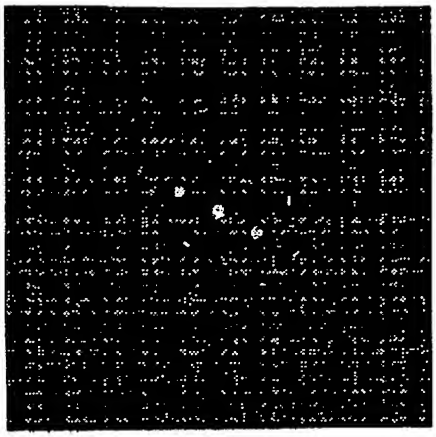
[Drawing 21]

図面代用写真

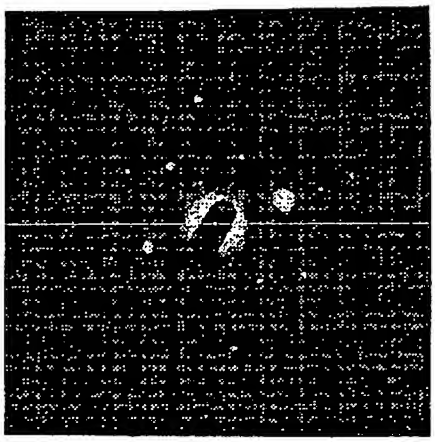


[Drawing 22]

図面代用写真



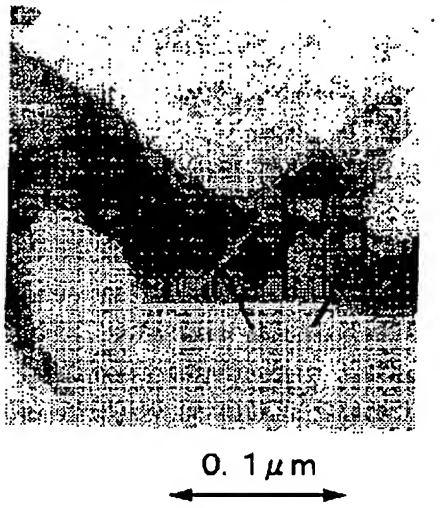
(a)



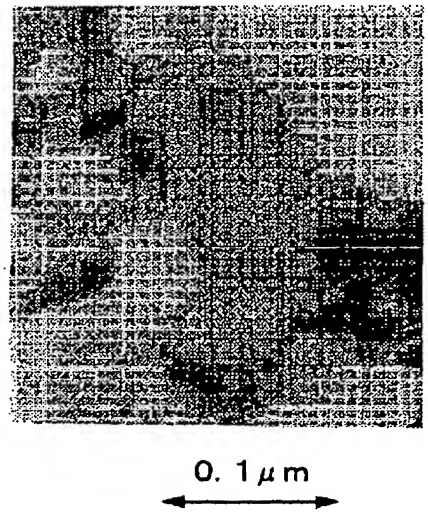
(b)

[Drawing 23]

図面代用写真



(a)



(b)

[Translation done.]